APS12OS

Application Module Supporting Freescale S12 Microcontrollers

For use with the following part numbers:

APS12OS-C128
APS12OS-DT256
APS12OS-XDT512

Board Marking:
APS12OS

USER GUIDE

Email: www.axman.com
Support: support@axman.com

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Revision History

Date	Rev	Comments
June 4, 2014	A	Initial Release
June 5, 2014	B	Removed extraneous TWR-S12G128 reference

CAUTIONARY NOTES

1) Apply Electrostatic Discharge (ESD) prevention measures when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; nor does it convey any license under patent rights or the rights of others.

3) EMC Information on the application module:

   a) This product is designed to comply with FCC requirements as a Class B device; however, this device is not tested for compliance. The user is responsible for ensuring this product does not cause undue interference with other electronic devices.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate preventive measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may affect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development module applies option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed - jumper is installed such that 2 pins are connected together

Jumper off, out, or idle - jumper is installed only on 1 pin or is removed completely. It is recommended that jumpers be idled by installing on 1 pin so they will not be lost.

Project Board – Optional component providing a common expansion and prototyping platform to enhance the learning experience, it supports multiple microcontroller application modules.

Application Module – A microcontroller development board, which features a Freescale Microcontroller.

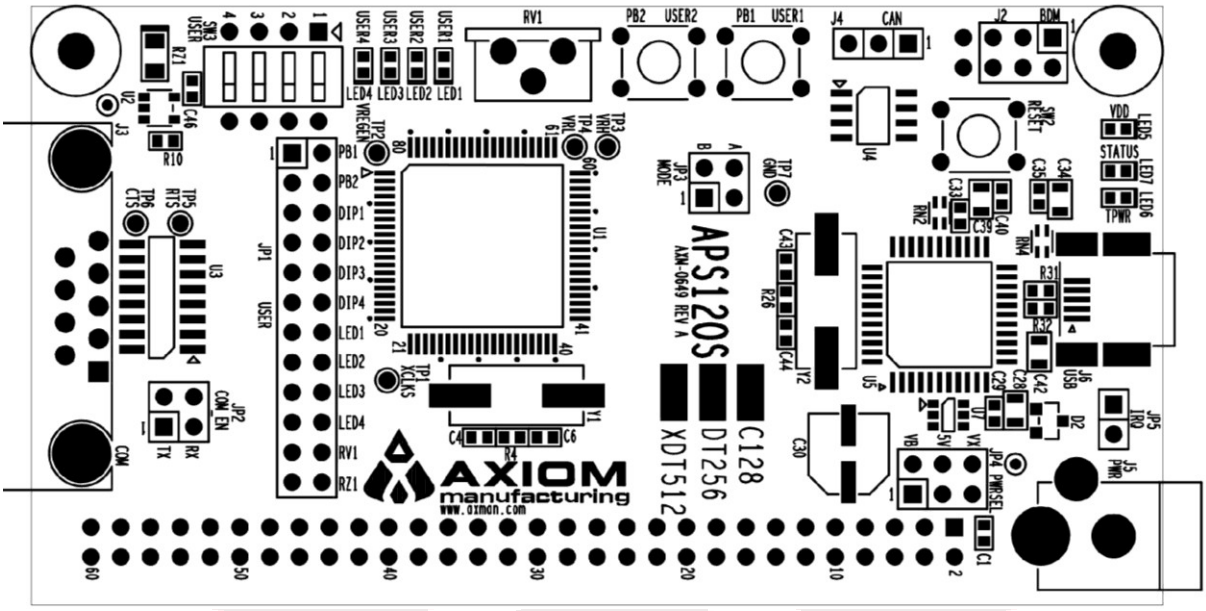
ABOUT THE APPLICATION MODULE

The APS12OS is an embedded application module targeted to educational use. This module supports the Freescale MC9S12C128, the MC9S12DT256 or the MC9S12XDT512 microcontrollers. These MCUs target a variety of automotive applications, featuring support for Byte Data Link Controller (BDLC), CAN, PWM, and I2C. The APS12OS applies an integrated OSBDM supporting quick and easy firmware (FW) development out of the box. A 60-pin connector allows the APS12Os to connect to the Microcontroller Project Board Student Learning Kit (PBMCUSLK) or to the user's custom PCB.

Installed Target Device

Topside markings show, which of the 3 supported MCUs, is installed. Only 1 MCU may be installed and will be clearly marked as described in the figure below.

Figure 1: APS12OS Top View



FEATURES

- MC9S12 C128/DT256/XDT512 MCU, 80 LQFP
  - 128/256/512 KB Flash EEPROM
  - 4KB EEPROM
  - Up to 32KB RAM
  - SAE J1850 Byte Data Link Controller
  - 8-ch, 10-bit, ATD w/ external trigger
  - 8-bit Enhanced Capture Timer with IC, OC, and Pulse Accumulate capabilities
  - 7-ch, 8-bit PWM
  - 9 KBI inputs
  - 56 GPIO
  - Up to 3 CAN Channels
  - CAN 2.0 A/B PHY w/ 3-pos header
  - 2 SCI & 2 SPI Channels
  - 1 IIC Channel
- RS-232 transceiver w/ DB9 connector
- 4 MHz Clock Oscillator
- Internal Power-On Reset Controller
- Internal Low Voltage Reset Controller
- Optional External Reset Supervisor (not installed)
- Power Input Selection Header
- On-board 5V regulator
- Optional power Input / Output from Connector J1
- User Components Provided
  - 1 DIP Switch, 4-pos
  - 3 Push Button Switches: 2 User, RESET
  - 5 LED Indicators: 4 User, +5V
- Option Headers
  - USER_EN
  - PWR_SEL
  - COM_EN
  - MODE (not installed)
- Connectors
  - 60-pos pin-header providing access to MCU IO signals
  - 2.0mm barrel connector power input
  - 6-pin BDM interface connector
  - 3-pos CAN interface connector
  - DB9 connector
- Supplied with DB9 Serial Cable and USB cable

Specifications:
Module Size 3.8” x 2.0”
Power Input: +9V typical, +6V to +18

REFERENCES

The latest product information, updates and reference documents can be found at www.freescale.com and/or www.axman.com

APS12OS_UG.pdf	APS12OS User Guide (this document)
AX-SCH-0649A.pdf	Application Module Schematic
MC9S12C128V1.pdf	MC912C128 Reference Manual
9S12DT256DGV3.pdf	MC9S12DT256 Reference Manual
9S12XDP512DGV2.pdf	MC9S12XDT512 Reference Manual

NOTE:
Microcontroller specific documentation such as memory map, register contents and description, and datasheets may be downloaded from www.freescale.com.

Current product information, reference materials, and updates may be downloaded from www.freescale.com/universityprograms.

GETTING STARTED

Please refer to the Quick Start Users Guide to quickly setup and getting started using the stand-alone application module or with the Freescale Project Board/Application Module

NOTE

Please refer to the Quick Start Guide for an illustrated guide to connecting the USB, and getting started with CodeWarrior.

DEVELOPMENT SUPPORT

Software Development

Software development requires the use of an HCS12 assembler or compiler and a host PC operating a debug interface. CodeWarrior Development Studio for S12(X), Ver. 5.1 provides a fully integrated development environment offering code editing, compilation, programming and debugging of Freescale Semiconductors. Users can program in C/C++ and in-line Assembly using CodeWarrior.

CodeWarrior Development Studio for S12(X) Special Edition may be downloaded from www.freescale.com at no cost. Although size constrained to 128kb, the Special Edition will support most development projects.

Device Memory Map

This application module is designed to support multiple HCS12 family microcontrollers specifically the MC9S12C, MC9S12DT, and MC9S12XDT family of MCU's. This section shows the default memory map for each MCU immediately out of reset. Refer to the specific MCU Reference Manual (RM) for further details.

Table 1: C128 Memory Map

0x0000 – 0x03FF	Registers	1K bytes	May be mapped to any 2K boundary
0x0400 – 0x2FFF	EEPROM	16K bytes	Fixed Flash EEPROM
0x3000 – 0x3FFF	RAM	4K bytes	May be mapped to any 4K boundary
0x4000 – 0x7FFF	Fixed FLASH	16K bytes	
0x8000 – 0xBFFF	Paged FLASH	128K bytes	16K Page Window, 8 pages
0xC000 – 0xFEFF	Fixed Flash	16K bytes	
0xFF00 – 0xFFFF	Vectors	256 bytes	BDM if active

Table 2: DT256 Memory Map

0x0000 – 0x03FF	Registers	1K bytes	May be mapped to any 2K boundary in the first 32K
0x0400 – 0x0FFF	EEPROM	4K bytes	May be mapped to any 4K block. Bottom 1K used by Registers out of reset
0x1000 – 0x3FFF	RAM	12K bytes	May be mapped to any 16K block and may be aligned top or bottom
0x4000 – 0x7FFF	Fixed FLASH	16K bytes	Dependant on state of ROMHM bit
0x8000 – 0xBFFF	Paged FLASH	256K bytes	16K Page Window, 16 pages
0xC000 – 0xFEFF	Fixed Flash	16K bytes	
0xFF00 – 0xFFFF	Vectors	256 bytes	BDM if active

NOTE: The bottom 1K of EEPROM is covered by registers out of reset.

Table 3: XDT512 Memory Map

0x0000 – 0x07FF	Registers	2 K bytes	
0x0800 – 0x0BFF	Paged EEPROM	4K bytes	4 – 1Kb pages
0x0C00 – 0x0FFF	Fixed EEPROM	1K bytes	
0x1000 – 0x1FFF	Paged RAM	20 KB	5 – 4Kb pages
0x2000 – 0x3FFF	Fixed RAM	8K bytes	
0x4000 – 0x7FFF	FIXED FLASH	16 KB	1K, 2K, 4K, 8K Protected Boot Sector
0x8000 – 0xBFFF	Paged FLASH	512K bytes	16K Page Window, 32 pages
0xC000 – 0xFEFF	FIXED FLASH	16 KB	2K, 4K, 8K, 16K Protected Boot Sector
0xFF00 – 0xFFFF	Vectors	255 bits	

Integrated OSBDM

An integrated Open-Source Background Debug Mode (OSBDM) supports quick and easy application development and debug without the requirement of an external debugger. However, a BDM header supports the use of external debuggers providing capabilities not supported by the OSBDM. CodeWarrior fully supports the OSBDM connection and provides direct, non-intrusive access to the target device internals. While in BDM mode, no internal resources are used. Code stepping and break points are fully supported.

Connection between a host PC and the target device is provided via a mini-B, USB connector. The OSBDM is capable of providing power to the target board eliminating the need for external power. Please note that power supplied by the OSBDM is limited by the USB specification. When powered through the OSBDM, total current draw, including the target module and any connected circuitry, must remain less than 300mA. Otherwise, the USB bus will cause the host PC to disconnect the board. Damage to the host PC, target board, or Tower System may result if this current limit is violated.

CAUTION:

When powered from the USB bus, do not exceed the 500mA maximum current drain allowed under the USB specification. Damage to the target board or host PC may result

OSBDM Bootloader

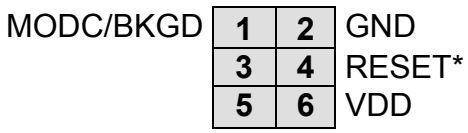
The OSBDM is pre-programmed with a bootloader application to allow field updates. The USB bootloader communicates with a GUI application running on a host PC. The GUI application allows the user to update

OSBDM firmware easily and quickly. Option jumper JP5 enables the bootloader at startup. This option header is not populated in default configuration. Refer to Freescale Application Note AN3561 for details on using the GUI application and bootloader. The application note may be found at www.freescale.com or at www.axman.com/support.

BDM_PORT Header

A 6-pin BDM port header allows connection of an external HC(S)12 compatible BDM cable for application development. Refer to the BDM cable documentation for details on use of the BDM cable with this module. This option is added for user convenience if needed.

Figure 2: BDM_PORT



See the HC12 Reference Manual for complete DEBUG documentation

Note: The BDM_PORT header is not installed in default configurations.

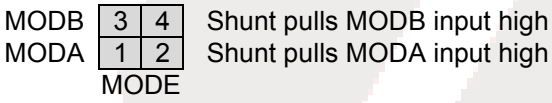
Expanded Bus Operation

The APS12OSC128 and APS12OSDT256 modules both support expanded mode operation. The user may access all multiplexed bus signals at connector J1. The APS12OSXDT512 does not support expanded bus mode. The MODE option header is used to configure the module for expanded bus mode operation. Refer to the target device Reference Manual for details on implementing the expanded bus.

Mode

By default, the applied microcontroller is configured for single-chip operation. The MODE option header allows the user to configure the board for expanded bus operation. In default configuration, this header is not installed.

Figure 3: MODE Option Header



NOTE: Expanded bus mode operation is supported only when a 9S12C128 or 9S12DT256 MCU is installed on the MCU.

NOTE: The Mode option header is not installed in default configurations.

POWER

Power may be applied to the APS12OS through 3 distinct connections. The module may be power via the integrated USB BDM, the barrel connector, or through connector J1. The following section describes the various power options and proper configuration.

Refer to Figure 4 below for details on configuring power input.

CAUTION

DO NOT apply power from multiple sources concurrently; otherwise, damage may result

Integrated USB Power Input

The APS12Os is designed to draw power from the integrated USB BDM. This feature supports quick and easy application development and debug. The BDM is configured to provide a maximum of 300mA of power to the module from the USB bus. The user must ensure this limit is not exceeded; otherwise, the host PC may disconnect the USB bus forcing a target device reset. Damage to the module or the host PC may also result. Total power consumption must include the module and any external circuitry connected to the IO header at J1.

Barrel Connector Power Input

The on-board voltage regulator (VR1) accepts power input through a 2.0mm, center-positive, barrel connector (PWR). Input voltage may range from +6V to +18V. The voltage regulator (VR1) provides a +5V fixed output voltage with current output limited to 250mA. Over-temperature and over-current limit built into the voltage regulator provide protection from excessive stresses. Do not exceed the maximum output current limit of VR1 when attempting to power off-board circuitry through connector J1.

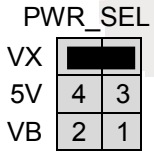
MCU_PORT Connector Power Input

The application module may be powered through the MCU_PORT connector at J1. Optionally, the APS12OS can supply power to the MCU_PORT at J1. These features simplify using the APS12OS in embedded applications

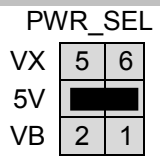
Power Select

The PWRSEL option header at JP4 allows the user to configure input power select. This option header allows selection between input power from the OSBDM, barrel connector, or connector J1. Exercise caution when using this select header. Enabling 2 or more power input options concurrently may damage the module.

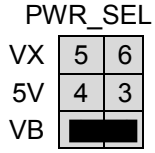
Figure 4: PWR_SEL Option Header



Source power from connect J1.
Optional: Source power to circuitry connected to J1 (requires 2nd shunt)



Source power input from barrel connector PWR.



Source power input from USB.

NOTE: Exercise caution when configuring this selection header. Improper configuration may damage the module.

RESET

The APS12OS module applies various RESET sources to ensure proper MCU operation. An optional external Reset Supervisor may also be installed for added robustness. Sufficient bias is applied to the RESET* signal ensuring normal MCU operation, added shunt capacitance ensures an adequate input pulse width and debounces the RESET switch.

Power-On RESET (POR)

Each target MCU applies an internal power on RESET (POR) to ensure proper device operation. The POR circuit holds the device in RESET until all input voltages stabilize at normal levels. Once input power stabilizes, the POR circuit releases RESET after a set period has elapsed.

Low Voltage RESET

Each target MCU applies an internal low-voltage reset circuit (LVR) to protect the MCU during brownout conditions. The LVR circuit ensures the device resets properly if input voltage falls below the trigger level. The LVR releases RESET a set period after input voltage return to normal level.

RESET Switch

The RESET switch provides a method to apply an asynchronous RESET to the MCU and connects directly to the RESET* signal on the applied MCU. Pressing the RESET switch applies a low voltage level to the RESET* input. This RESET input triggers the POR circuit, which asserts RESET for a set period after switch release.

External RESET Supervisor

The APS12OS supports installation of an optional RESET supervisor. The Maxim Integrated, DS1813 may be installed at location LV1 if needed for added robustness. The DS1813 provides tighter regulation of POR and LVR functions along with a 150 ms RESET period. Refer to the DS1813 datasheet for details on use and operation.

TIMING

Timing input to the MCU is provided by a 4 MHz, fundamental frequency crystal oscillator. The oscillator exhibits a frequency tolerance of ±30ppm. The timing input is configured for full-swing Pierce mode operation in all MCU configurations.

The XCLKS output is routed to test point VIA located near the MCU. The internal clock ECLKX2 is available at this via if needed.

COMMUNICATIONS

The APS12OS module provides the user with 1, RS-232 COM port and 1, high-speed CAN port on the module. The RS-232 port, COM1, connects to SCI0 on the MCU. The RS-232 channel is configured as a DCE device. This allows a straight through cable between the module and the host PC. Suitable physical layer interfaces (PHY) are applied supporting both RS-232 and CAN signaling.

Additionally, the MCU may support up to 2 additional CAN ports, 2 SPI ports, and 1I2C port depending on the MCU installed. Access to these communications ports is provided at connector J1. Physical layer support is not provided for these features and must be provided by the user if needed.

RS-232

An RS-232 translator provides RS-232 to TTL/CMOS logic level translation on the COM connector, which consists of a 9-pin Dsub, right-angle connector. A ferrite bead on shield ground provides conducted immunity protection. Communication signals TXD and RXD are routed from the transceiver to the MCU. Communications signals TXD and RXD also connect to general purpose Port S signals on the MCU. Access to logic signals RTS and CTS are provided by vias located adjacent to the RS-232 PHY at U3.

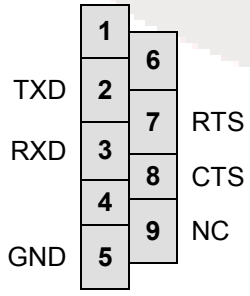
Table 4: COM Connections

MCU Port	COM Signal	I/O PORT CONNECTOR
PS1/TXD0	TXD0	J1-5
PS0/RXD0	RXD1	J1-7

COM Connector

A standard 9-pin D-sub connector provides external connection for COM1. The D-sub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. The figure below details the DB9 connector.

Figure 5: COM Connector



A female DB9 connector attached to the MCU internal SCI0 serial port via the RS232 transceiver. It provides simple 2 wire asynchronous serial communications without flow control. Flow control is provided at test points on the board. A straight-through cable is used to connect the module to a DTE device such as a host PC.

Pins 1, 4, and 6 are connected together.

Communications signals TxD/RxD also route to connector J1 for use off-module. When using these signals to drive off-module RS-232 devices the user should disconnect the on-board RS-232 transceiver. The COM_EN header block allows the user connect or disconnect the RS-232 transceiver.

Figure 6: COM_EN Header

Selects and enables serial communications through COM connector. Remove jumpers to disable on-board RS-232 transceiver.

MSCAN

The application module applies the TJA1040, high-speed CAN physical interface. A 3-pin connector provides connectivity to the off-board CAN bus. The CAN PHY connects to the MCU CAN0 channel. The PHY supports data rates up to 1 Mbps with slew-rate control. The figure below shows the pin-out of the CAN_PORT connector. Refer to the TJA1040 datasheet for details on use and configuration.

Figure 7: CAN_PORT Connector

1	CAN_H	The CAN PHY connects to the CAN0 channel in the MCU
2	GND	
3	CAN_L	

The installed MCU may provide support for additional CAN channels. All CAN channels supported are routed to the connector J1 for use if needed. Consult the relevant Device User Guide for the installed MCU for further details.

VRH/VRL

Voltage inputs VRH and VRL provide the upper and lower reference inputs for the analog to digital (ATD) converter. By default, VRH is tied to VDD and VRL is tied to ground. Adequate filtering has been added to provide a voltage reference with minimal ripple. Either, or both, references may be isolated to provide alternate ATD input references. A test point via on each signal, labeled VRH, or VRL, provides an easy way to attach an alternate reference voltage.

A 0-ohm configuration resistor allows the user to isolate each reference voltage. Removing R6 isolates VRH while removing R7 isolates VRL. Install suitably sized 0-ohm resistors in these locations to restore the board to its default configuration.

Care must be exercised when using alternate input references. The associated configuration resistor must be removed before applying an alternate voltage reference or the board may be damaged. In addition, no input protection is provided; incorrect configuration will damage the MCU. The table below summarizes the changes necessary to use alternate VRH and/or VRL.

Table 5: ATD Reference Voltage

	Installed (Default)	Removed
R6	VRH = VDD	VRH provided by user
R7	VRL = GND	VRL provided by user

NOTE: Damage to the board may result if an alternate reference voltage is attached without first removing the associated configuration resistor.

USER I/O

User I/O includes 2 push button switches, one 4-position DIP switch, 4 green LEDs, a potentiometer, and a photo-sensor. The sections below provide details on each User I/O. The User option header block enables or disables each User I/O individually.

Before applying any USER I/O function, the user must configure each MCU pin as to direction and type. Refer to the target MCU Reference Manual for details on configuration and usage.

Table 6 below details connections applied to each User I/O, while Table 7 shows jumper settings to enable and disable each User I/O.

Switches

The application module applies 2 push-button switches and one 4-position DIP switch for user input. Each switch is configured for active-low operation. To ensure proper operation, the user must enable the target MCU internal pull-up resistors before using any switch input. Each switch connection must be configured as a general-purpose input.

Both push-button switches are normally-open (NO) in the default position. Pressing the switch button closes the circuit, applying a low input level on the associated MCU signal pin. Use of the target MCU internal pull-up ensures proper signal bias allowing the MCU to read the correct input level. Both push-button switches connect to Key-Wakeup (KW) inputs on the target MCU. To use the KW functionality, user FW should adequately debounce the input signal to remove spurious transients created during the switch press and release.

Each DIP switch position provides bi-stable operation. The OFF position opens the switch contacts while the ON position closes the switch contacts and applies a low input level on the associated MCU input. Use of the target MCU internal pull-up ensures proper signal bias allowing the MCU to read the correct input level

LEDs

The application module provides 4 green LEDs for output indication. Each LED is configured for active low operation. A current-limit resistor prevents excessive diode current. Turn each LED ON by configuring the associated MCU pin as an output and writing a logic low. It is good practice to set the output logic level before configuring the pin direction, preventing spurious output behavior. Turn each LED OFF by writing a logic high or configuring the pin as an input.

POT

A single-turn, 5K ohm trimmer potentiometer (POT) is applied to simulate analog input. A decoupling capacitor minimizes noise and smoothes transitions during adjustment. Configure the associated MCU pin as an analog input to use this feature.

Light Sensor

The APS12OS applies a light sensor exhibiting 23K – 33K ohms of output resistance. Sensor output resistance and voltage applied to the target MCU input is inversely related to incident light intensity. A gain stage (U5) amplifies the sensor output before connecting to the MCU. The SENSOR connects to analog input PAD04/AN04 on the MCU. The associated MCU pin must be configured for analog input to use this feature.

User I/O MCU Signals

The following table shows the connection for each user I/O device.

Table 6: User I/O Signal Assignment

USER	Ref Des	Signal	Description
1	PB1	PP0/KWP0	Push Button Switch 1
2	PB2	PP1/KWP1	Push Button Switch 2
3	DIP1	PB0	DIP Switch 1
4	DIP2	PB1	DIP Switch
5	DIP3	PB2	DIP Switch
6	DIP4	PB3	DIP Switch
7	LED1	PB4	Green LED
8	LED2	PB5	Green LED
9	LED3	PB6	Green LED
10	LED4	PB7	Green LED
11	RV1	PAD05/AN05	Potentiometer
12	RZ1	PAD04/AN04	Light Sensor

User Option Enables

The User option header block enables or disables each User I/O individually. User I/O includes 4 green LEDs, 2 push-button switches, one 4-position DIP switch, a light sensor, and a potentiometer. Installing a shunt enables the associated option. Removing a shunt disables the associated option. The table below shows the configuration option for each USER I/O.

Table 7: USER Option Header

			Shunt		
	USER		Installed	Removed	Description
PB1	**1**	**2**	Enable	Disable	Push Button Switch 1
PB2	**3**	**4**	Enable	Disable	Push Button Switch 2
DIP1	**5**	**6**	Enable	Disable	DIP Switch 1
DIP2	**7**	**8**	Enable	Disable	DIP Switch
DIP3	**9**	**10**	Enable	Disable	DIP Switch
DIP4	**11**	**12**	Enable	Disable	DIP Switch
LED1	**13**	**14**	Enable	Disable	Green LED
LED2	**15**	**16**	Enable	Disable	Green LED
LED3	**17**	**18**	Enable	Disable	Green LED
LED4	**19**	**20**	Enable	Disable	Green LED
RV1	**21**	**22**	Enable	Disable	Potentiometer
RZ1	**23**	**24**	Enable	Disable	Light Sensor

MCU_PORT I/O

Connector J1 provides access to the MCU I/O signals. Only signal XCLS is not available at this connector.

Figure 8: MCU_PORT Connector, J1

V_{AUX}	1	2	PE1/IRQ*
GND	3	4	RESET*
PS1/TXD0	5	6	MODC/BKGD
PS0/RXD0	7	8	PP7/KWP7/PWM7/SCK2
PP0/KWP0/PWM0/MISO1	9	10	PAD07/AN07
PP1/KWP1/PWM1/MOSI1	11	12	PAD06/AN06
PT0/IOC0	13	14	PAD05/AN05
PT1/IOC1	15	16	PAD04/AN04
PM4/RXCAN2/RXCAN0/RXCAN4/MOSI0	17	18	PAD00/AN00
PM2/RXCAN1/RXCAN0/MISO0	19	20	PAD01/AN01
PM5/TXCN2/TXCAN0/TXCAN4/SCK0	21	22	PAD02/AN02
PM3/TXCAN1/TXCAN0/SS0*	23	24	PAD03/AN03
PA7/*ADDR15*/*DATA15*	25	26	PJ7/KWJ7/TXCAN4/SCL0
PA6/*ADDR14*/*DATA14*	27	28	PJ6/KWJ6/RXCAN4/SDA0
PA5/*ADDR13*/*DATA13*	29	30	PP2/KPP2/PWM2/SCK1
PA4/*ADDR12*/*DATA12*	31	32	PP3/KWP3/PWM3/SS1*
PA3/*ADDR11*/*DATA11*	33	34	PP4/KWP4/PWM4/MISO2
PA2/*ADDR10*/*DATA10*	35	36	PP5/KWP5/PWM5/MOSI2
PA1/*ADDR9*/*DATA9*	37	38	PS2/RXD1
PA0/*ADDR8*/*DATA8*	39	40	PS3/TXD1
PB7/*ADDR7*/*DATA7*	41	42	PE0/XIRQ*
PB6/*ADDR6*/*DATA6*	43	44	PE2/*RW*
PB5/*ADDR5*/*DATA5*	45	46	PE3/*LSTRB**
PB4/*ADDR4*/*DATA4*	47	48	PE4/*ECLK*
PB3/*ADDR3*/*DATA3*	49	50	PT2/IOC2
PB2/*ADDR2*/*DATA2*	51	52	PT3/IOC3
PB1/*ADDR1*/*DATA1*	53	54	PT4/IOC4
PB0/*ADDR0*/*DATA0*	55	56	PT5/IOC5
PM1/TXCAN0/*TXB*	57	58	PT6/IOC6
PM0/RXCAN0/*RXB*	59	60	PT7/IOC7