TWR-S12GN32

Demonstration Board for Freescale MC9S12GN32 Microcontroller

USER GUIDE

Web Site: www.axman.com
Support: support@axman.com

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REVISION

Date	Rev	Comments
August 16, 2010	A	Initial Release
January 4, 2011	B	Removed OSBDM disclaimer, removed MSCAN reference, corrected connector reference designators, minor format updates

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the TWR-S12GN32 board:

   a) This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may affect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development module utilizes option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

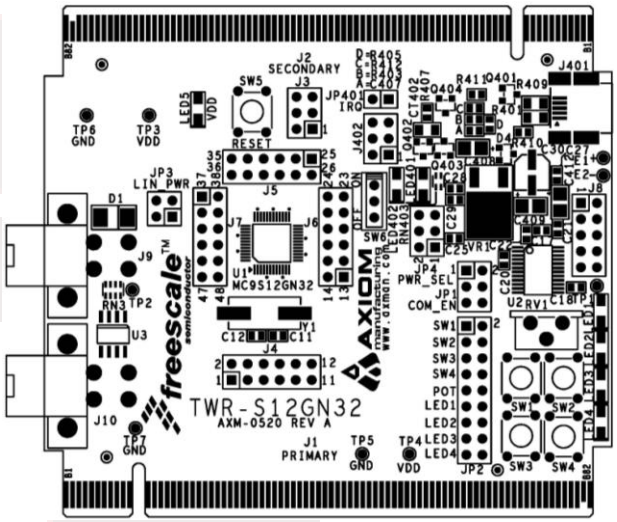
Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Signal names followed by an asterisk (*) denote active-low signals.

FEATURES

The TWR-S12GN32 is a demonstration board for the MC9S12GN32 microcontroller; an automotive, a low-cost, high-performance, 16-bit microcontroller in a low pin-count device. The MC9S12GN32 provides16-bit wide accesses, without wait states, for all peripheral accesses. The MC9S12GN32 targets automotive applications requiring LIN/J2602 communications. Examples include body controllers, occupant detection, etc…

The board is designed to interface to the Freescale Tower System, a modular development platform which aids in rapid prototyping and tool-reuse. An integrated Open-Source BDM, software tools, and examples provided with the development board make application development and debug quick and easy. All MCU signals are available on one or both edge connectors. An IO ring around the MCU also provided easy access to all signals.



- MC9S12GN32, 48 LQFP
  - 32K Bytes Flash
  - 1024 Bytes EEPROM
  - 2048 Bytes RAM
  - 25MHz Bus Frequency
  - Internal Oscillator
  - SCI, SPI
- Integrated Open Source BDM (OSBDM)
- BDM_PORT header for external BDM cable support
- 1 ea, Enhanced LIN Physical Layer Transceiver
- RS-232 Serial Data Physical Layer Transceiver
- On-board +5V regulator
- Power input from OSBDM, Tower System, or input vias at E1/E2
- Power Input Selection Jumpers
  - Power input from Integrated OSBDM
  - Power input from on-board regulator
  - Power input from LIN connectors
  - Power input from Tower System edge connector
- Peripherals
  - 5 Push Button Switches, 4 User, 1 Reset
  - 7 LED Indicators, 4 User, 2 OSBDM, 1 Power
  - 5K ohm POT w /LP Filter
- User Option Jumpers to disconnect Peripherals
- Connectors
  - 2x3 BDM_PORT Connector for External BDM Cable
  - USB mini-AB Connector for OSBDM
  - 2x5, 0.1” ctr, RS-232 Header

Specifications:

Board Size: 3.55” x 3.20” overall

Power Input: +7VDC ≥ V_{IN} ≥ 27VDC if supplied from LIN BUS or E1 / E2 input or +5VDC from USB connector or from Tower System
NOTE: LIN functionality requires V_{IN} ≥ +12V

MEMORY MAP

Figure 1 below shows the memory map for the MC9S12GN32. Refer to the MC9S12G Family Reference Manual (RM) for information on use and configuration of internal peripherals.

Figure 1: Memory Map

Address	Module	Size (Bytes)
0x0000 – 0x0009	PIM (port integration module)	10
0x000A – 0x000B	MMC (memory map control)	2
0x000C – 0x000D	PIM (port integration module)	2
0x000E – 0x000F	Reserved	2
0x0010 – 0x0017	MMC (memory map control)	8
0x0018 – 0x0019	Reserved	2
0x001A – 0x001B	Device ID register	2
0x001C – 0x001F	PIM (port integration module)	4
0x0020 – 0x002F	DBG (debug module)	16
0x0030 – 0x0033	Reserved	4
0x0034 – 0x003F	CPMU (clock and power management)	12
0x0040 – 0x006F	TIM0 (timer module)	48
0x0070 – 0x009F	ATD (analog-to-digital converter, 10 bit, 8-channel)	48
0x00A0 – 0x00C7	PWM (pulse-width modulator)	40
0x00C8 – 0x00CF	SCI0 (serial communications interface)	8
0x00D0 – 0x00D7	Reserved	8
0x00D8 – 0x00DF	SPI0 (Serial Peripheral Interface)	8
0x00E0 – 0x00E7	Reserved	8
0x00E8 – 0x00EF	Reserved	8
0x00F0 – 0x00F7	Reserved	8
0x00F8 – 0x00FF	Reserved	8
0x0100 – 0x0113	FTMRG control registers	20
0x0114 – 0x011F	Reserved	12
0x0120	INT (interrupt module)	1
0x0121 – 0x013F	Reserved	31
0x0140 – 0x017F	Reserved	64
0x0180 – 0x023F	Reserved	192
0x0240 – 0x025F	PIM (port integration module)	64
0x0260 – 0x0261	ACMP (Analog Comparator)	2
0x0262 – 0x275	PIM (port integration module)	20
0x0276	Reserved	1
0x0277 – 0x0x7F	PIM (port integration module)	9
0x0280 – 0x02EF	Reserved	112
0x02F0 – 0x02FF	CPMU (clock and power management)	16
0x0300 – 0x03FF	Reserved	256

SOFTWARE DEVELOPMENT

Software development requires the use of a compiler or an assembler supporting the HCS12(X) instruction set and a host PC running a debug interface. CodeWarrior Development Studio is supplied with this board for application development and debug. Refer to the supporting CodeWarrior documentation for details on use and capabilities.

DEVELOPMENT SUPPORT

Application development and debug for the target TWR-S12GN32 board is supported through the Open-Source Background Debug Mode (OSBDM) interface or an external BDM interface connector. The OSBDM is fully supported in CodeWarrior and provides direct, non-intrusive access to the target device internals. While in BDM mode, no internal resources are used. Code stepping and break-points are fully supported.

Connection between a host PC and the target device is provided via a mini-B, USB connector. The OSBDM is capable of providing power to the target board eliminating the need for external power. Please note that power supplied by the OSBDM is limited by the USB specification. When powered through the OSBDM, total current draw, including the OSBDM, TWR-S12GN board, and Tower System must remain less that 500mA. Otherwise, the USB bus will cause the host PC to disconnect the board. Damage to the host PC, target board, or Tower System may result if this current limit is violated.

CAUTION:

When powered from the USB bus, do not exceed the 500mA maximum current drain allowed by the USB specification.

Damage to the target board or host PC may result otherwise

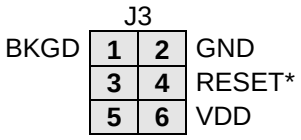
OSBDM Bootloader

The OSBDM is pre-programmed with a bootloader application to allow field updates of the OSBDM firmware (FW). The USB bootloader communicates with a GUI application running on a host PC. The GUI application allows the user to update OSBDM firmware quickly and easily. Option jumper JP401 enables the bootloader at startup. This option header is not populated in default configuration. Refer to Freescale Application Note AN3561 for details on using the GUI application and bootloader. The application note may be found at www.freescale.com.

BDM_PORT Header

A 6-pin header at J3 supports the use of external, S12 compatible, BDM cables. Refer to the external programming/debug cable documentation for details on use. Figure 2 below shows the pin-out for the BDM_PORT header.

Figure 2: BDM_PORT Header



See the associated RM for complete DEBUG documentation

POWER

The TWR-S12GN board may be powered from the OSBDM, from the Tower System elevator, from the LIN +V input, or 2 input vias at E1 & E2. The LIN +V input accepts +12V from the LIN bus and uses an on-board regulator to create the board operating voltage. Input vias at E1 & E2 allow connecting external power to the board if desired. An on-board regulator is used to create the board operating voltage from this input.

Use of the on-board regulator requires input voltage between +7.V and +27V. However, input voltage should be kept as low as possible to reduce excessive self-heating of the regulator.

CAUTION:

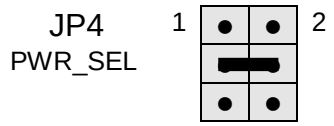
This board does not apply reverse polarity or transient protection on inputs E1 & E2. Polarity for each input is clearly marked.

Reverse input polarity on these inputs will damage the board.

Power Select

The option header, PWR_SEL, selects the input power source for the target board. When powered from the Tower System, the OSBDM voltage output is disabled. Figure 3 below shows the selection setting for each shunt position.

Figure 3: PWR_SEL Option Header



Select TWR voltage input
Select OSBDM voltage input (default)
Select on-board regulator input

RESET

The MC9S12GN32 provides several sources of reset internally. The internal reset circuitry negates the need for external reset input. The following sections provide an overview of external sources of reset. The MC9S12GN32 supports other sources of RESET. The MC9S12G Family Reference Manual provides further details on use and configuration of the S12CPMU.

Power-On Reset

The internal Power-On Reset (POR) circuit holds the MC9S12GN32 in reset until power has stabilized. While VDD input is rising, the POR circuitry holds the MCU in reset. After power has reached nominal levels, the POR circuitry fetches the associated reset vector.

Low Voltage Reset

The MC9S12GN32 applies an internal Low Voltage Reset (LVR) circuit to ensure proper device operation. In the event power input on VDD, VDDX, or VDDF falls below a pre-defined voltage level. The POR circuit holds the MCU in reset until input voltage rises to nominal levels.

Reset Switch

The RESET switch input allows the user to apply an asynchronous reset input to the MC9S12GN32 MCU. Upon detecting the reset input, the MCU drives the RESET* pin low for a pre-defined period. The RESET switch input is pulled-up to prevent spurious activation of the reset circuitry.

TIMING

By default, the MC9S12GN32 internal timing source is active out of RESET. An external 8MHz crystal oscillator, configured for low-power operation, is applies for applications requiring tight timing tolerance. The MC9S12G Family Reference Manual provides further details on use and configuration of the S12CPMU.

COMMUNICATIONS

Communications options for the TWR-S12GN32 include serial RS-232 and LIN. Serial RS-232 communications is supported through a RS-232 physical layer device (PHY) and a 2x5 pin header. An auxiliary 2x5 header to DB9 ribbon cable allows connection to the serial output connector.

A high-speed, enhanced, LIN PHY provides LIN bus communications through a 2x2 Molex connector. The LIN connector accepts cables built using Molex housing, pn 39-01-2040 and pins, pn 39-00-0217. The COM_SEL option header connects the MCU SCI signals to either the LIN PHY or the RS-232 PHY.

RS-232

The TWR-S12GN32 applies the MAX3387E, RS-232 physical-layer (PHY) transceiver to support serial communications. The PHY is configured for full handshaking. A standard 2x5 "Berg" pin-header on 0.1" centers and an IDC to DB9 cable supports connecting standard serial cables to the target board. Figure 4 below shows the SCI signal connections.

Optional control signals allow user application complete control over PHY operation. The FORCEOFF* input allows the user application to turn-off the PHY under MCU control for power savings. For normal operation, the user application should drive FORCEOFF* high. Alternatively, CT9 may be opened to allow the FORCEOFF* input to be pulled high.

The INVALID* output signal provides indication that no valid RS-232 signal is present. Figure 4 below shows the signal connections to the RS-232 transceiver.

Figure 4: Serial Connections

MCU Port Signal	Transceiver Signal	COM CONNECTOR	COMMENTS
	+5V	J5-1	
PS1//TXD0	TXD	J5-3	pull-up
PS0//RXD0	RXD	J5-5	
PM1/TXD1/*RXCAN*	DTR	J5-7	CT6 (NO)
PAD1/KWAD1/AN1	DSR	J5-2	pull-up
	GND	J5-9	
PAD2/KWAD2/AN2	CTS	J5-4	CT7 (NO), pull-up
PM0/RXD2/*RXCAN*	RTS	J5-6	pull-up
	TP2	J5-8	
PAD8/KWAD8/AN8	INVALID*		CT8 (NO)
PAD3/KWAD3/AN3	FORCEOFF*		CT9 (NC)

NOTE: For normal RS-232 operation, FORCEOFF* should be actively driven to the high level. Alternately, open CT9 to allow FORCEOFF* to float high.

NOTE: MSCAN is not supported on the MC9S12GN32 MCU. Reference to MSCAN in signal names above are included to correspond to the Device Reference Manual.

COM Connector

A 2x5, 0.1", standard "Berg" pin-header provides external connections for the SCI port. The supplied IDC to DB9 ribbon cable adapter allows the user of standard serial communications cables with the target board. Figure 5 below shows the COM1 pin-out. Figure 5 below shows the signal connections for the COM1 connector.

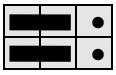
Figure 5: COM1 Connector

2, 7	1	2	1, 7
TXD	3	4	CTS
RXD	5	6	RTS
1, 2	7	8	TP2
GND	9	10	NC

COM_EN

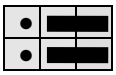
The COM_EN option header connects the MCU SCI port to either the SCI PHY or the LIN PHY. Figure 6 below shows the option jumper configuration for the COM_EN option header.

Figure 6: COM_EN Option Header



Connects target MCU SCI port to LIN PHY to enable LIN bus communications

COM_EN



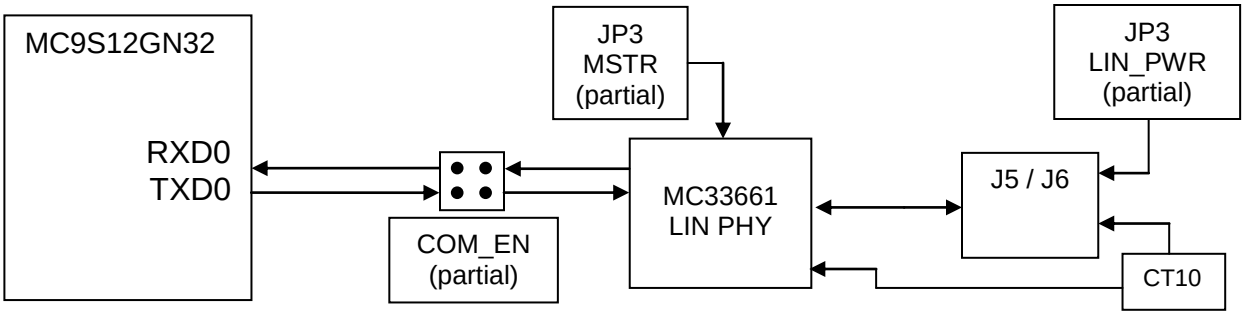
Connects target MCU SCI port to RS-232 PHY to enable serial communications (default)

COM_EN

LIN Port

The TWR-S12GN32 applies the MC33661 LIN bus physical layer device (transceiver) to support LIN communications. The PHY may be configured as a Master or Slave node on the LIN bus. LIN connectors J9 & J10 are configured in parallel to support pass-thru signaling. Figure 7 details the LIN block diagram.

Figure 7: LIN Block Diagram



The LIN interface provides optional features of slew rate control, network supply, and wake up option. Refer to the MC33661 Reference Manual for detail on PHY functionality. The following sections detail functionality for LIN option jumpers.

LIN Enable

The LIN PHY is enabled by default. Disable the PHY by connecting the test point, TP3, to GND.

LIN COM Input

LIN inputs RX and TX are enabled using the COM_EN option header. Refer to Figure 6 above for details on configuring this header.

LIN_PWR Option

The LIN_PWR option jumper connects pin 1 of both LIN connectors to the +V input. In Master mode, this option may be used to power LIN slave devices. This option requires +12V be applied at E1/E2 inputs. In Slave mode, this option allows slave device to draw power from the LIN network. For Slave mode configuration, external power should not be applied to the target board. LIN_PWR is enabled by installing a shunt from JP3-1 to JP3-2. Refer to Figure 8 below.

CAUTION:

If the target board draws power from the LIN bus in Slave mode, do not apply external power at E1/E2 inputs. Damage to the board may result.

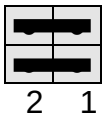
NOTE:

If the target board powers the LIN bus in Master mode, +12V must be applied externally at E1/E2 inputs.

MSTR Option

The MSTR option jumper allows the LIN transceiver to be configured for Master mode functionality. Master mode may also be set using the INH pin on the PHY. Refer to the MC33661 device datasheet for details on use and configuration. Refer to Figure 8 below.

Figure 8: JP3 Option Header



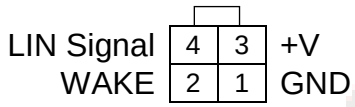
JP3 Connect LIN bus to +V input (default)
LIN_PWR Enables LIN Master mode functionality (default)

NOTE: LIN PHY may also be configured as a Master Node using the INH pin. Refer to the LIN PHY data sheet for details.

LIN-J1 Connector

The TWR-S12GN32 supports two, 2 x 2 Molex connectors to interface to the LIN bus. Figure 9 below details the pin-out of the LIN bus connector.

Figure 9: LIN Connector



Front View – Looking into Connector

NOTE: LIN Port Connector – Molex 39-29-1048
Mates with; Housing – Molex 39-01-2040, Pin – Molex 39-00-0036

USER PERIPHERALS

User I/O includes 1 potentiometer, 4 push button switches, and 4 green LEDs for user I/O. The USER (JP14) option header enables or disables each User I/O function individually. The sections below provide details on user I/O. Figure 10 below shows the USER jumper settings.

Potentiometer

The TWR-S12GN32 target board applies a single-turn, 5K, ohm potentiometer (POT) to simulate analog input. The POT is connected to an ATD input on the target MCU and is decoupled to minimize noise transients during adjustment. Figure 10 below shows the USER jumper settings.

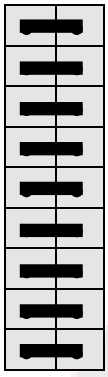
User LED's

The TWR-S12GN32 target board applies 4, green, LEDs for output indication. Each LED is configured for active-low operation. A series, current-limit resistor prevents excessive diode current. Each LED is connected to a timer channel output on the target MCU. Figure 10 below shows the USER jumper settings.

Pushbutton Switches

The TWR-S12GN32 provides 4 push-button switches for user input. Each push-button switch is configured for active-low operation and is connected to a key-wakeup input on the target MCU. External bias is applied to each switch input to ensure proper operation. Figure 10 below shows the USER jumper settings.

Figure 10: JP1 Option Header



JP1	Signal	ON	OFF
SW1	PAD4/KWAD4/AN4	Enabled	Disabled
SW2	PAD5/KWAD5/AN5	Enabled	Disabled
SW3	PAD6/KWAD6/AN6	Enabled	Disabled
SW4	PAD7/KWAD7/AN7	Enabled	Disabled
POT	PAD10/AN10/ACMP1	Enabled	Disabled
LED1	PT2/IOC2	Enabled	Disabled
LED2	PT3/IOC3	Enabled	Disabled
LED3	PT4/IOC4	Enabled	Disabled
LED4	PT5/IOC5	Enabled	Disabled

NOTE: User peripheral input/output is enabled by default.

IO RING PIN-OUT

An IO Ring on the TWR-S12GN32 provides convenient access to MCU signals. The IO ring is arranged as series of 2x12, 0.1" ctr, "Berg" style pin headers surrounding the MCU. The figures below show the pin-out for each IO ring header.

Figure 11: IO Ring Pin-Out

MCU PIN	Signal			Signal	MCU PIN
		J7			
1	RESET*	1	2	VDDR	2
3	NC	3	4	PE0	4
5	VSSX1	5	6	PE1	6
7	NC	7	8	PJ0/KWJ0/PWM6/MISO1	8
9	PJ1/KWJ1/IOC6/MOSI1	9	10	PJ2/KWJ2/IOC7/SCK1	10
11	PJ3/KWJ3/PWM7/SS1*	11	12	BKGD	12
		J8			
13	PP0/KWP0/ETRIG0/API_EXTCLK	1	2	PP1/KWP1/ETRIG1/EXTCLKX2	14
15	PP2/KWP2/ETRIG2/PWM2	3	4	PP3/KWP3/ETRIG3/PWM3	16
17	PP4/KWP4/PWM4	5	6	PP5/KWP5/PWM5	18
19	PT5/IOC5	7	8	PT4/IOC4	20
21	PT3/IOC3	9	10	PT2/IOC2	22
23	PT1/IOC1/IRQ*	11	12	PT0/IOC0/XIRQ*	24
		J9			
25	PAD0/KWAD0/AN0	1	2	PAD8/KWAD8/AN8	26
27	PAD1/KWAD1/AN1	3	4	PAD9/KWAD9/AN9/ACMPO	28
29	PAD2/KWAD2/AN2	5	6	PAD10/KWAD10/AN10/ACMPP	30
31	PAD3/KWAD3/AN3	7	8	PAD11/KWAD11/AN11/ACMPM	32
33	PAD4/KWAD4/AN4	9	10	PAD5/KWAD5/AN5	34
35	PAD6/KWAD6/AN6	11	12	PAD7/KWAD7/AN7	36
		J10			
37	VDDA	1	2	VSSA	38
39	PS0/RXD0	3	4	PS1/TXD0	40
41	PS2/RXD1	5	6	PS3/TXD1	42
43	PS4/MISO0	7	8	PS5/MOSI0	44
45	PS6/SCK0	9	10	PS7/API_EXTCLK/ECLK/SS0*	46
47	PM0/RXD2	11	12	PM1/TXD2	48

EDGE CONNECTOR PIN-OUT

The TWR-S12GN board connects to the Freescale Tower System using the 2 PCIe Edge Connectors. Following the PCIe specification, the Bx signals are located on the top of the board and the Ax signals are located on bottom. Pin B1 for the primary and secondary connectors are at opposite corners of the board. Figure 12 and Figure 13 below show the pin-out the primary and secondary edge connectors. Pin positions with no signal name shown are not connected.

Figure 12: Primary Edge Connector

Pri_B01	**5.0V Power**	Pri_A01	**5.0V Power**
Pri_B02	**Ground**	Pri_A02	**Ground**
Pri_B03		Pri_A03	
Pri_B04	Elevator Power Sense	Pri_A04	
Pri_B05	**Ground**	Pri_A05	**Ground**
Pri_B06	**Ground**	Pri_A06	**Ground**
Pri_B07	PT2/IOC2	Pri_A07	
Pri_B08		Pri_A08	
Pri_B09	PT1/IOC1/IRQ*	Pri_A09	
Pri_B10	PT0/IOC0/XIRQ*	Pri_A10	
Pri_B11	PAD0/KWAD0/AN0	Pri_A11	
Pri_B11A			
Pri_B12		Pri_A12	
Pri_B13		Pri_A13	
Pri_B14		Pri_A14	
Pri_B15		Pri_A15	
Pri_B16		Pri_A16	
Pri_B17		Pri_A17	
Pri_B18		Pri_A18	
Pri_B19		Pri_A19	
Pri_B20		Pri_A20	
Pri_B21		Pri_A21	
Pri_B22		Pri_A22	
Pri_B23		Pri_A23	
Pri_B24		Pri_A24	VDDR
Pri_B25		Pri_A25	VSSX
Pri_B26	**Ground**	Pri_A26	**Ground**
Pri_B27	PAD8/KWAD8/AN8	Pri_A27	PE0/EXTAL
Pri_B28	PAD1/KWAD1/AN1	Pri_A28	VSSX1
Pri_B29	PAD9/KWAD9/AN9/ACMPO	Pri_A29	PE1/XTAL
Pri_B30	PAD2/KWAD2/AN2	Pri_A30	TEST
Pri_B31	**Ground**	Pri_A31	**Ground**
Pri_B32		Pri_A32	
Pri_B33	PAD10/KWAD10/AN10/ACMPP	Pri_A33	PJ0/KWJ0/PWM6/MISO1
Pri_B34	PAD3/KWAD3/AN3	Pri_A34	PJ1/KWJ1/IOC6/MOSI1
Pri_B35		Pri_A35	

Pri_B36	**3.3V Power**	Pri_A36	**3.3V Power**
Pri_B37		Pri_A37	PJ2/KWJ2/IOC7/SCK1
Pri_B38		Pri_A38	Text
Pri_B39	PAD11/KWAD11/AN11/ACMPM	Pri_A39	PJ3/KWJ3/PWM7/SS1*
Pri_B40	PAD4/KWAD4/AN4	Pri_A40	BKGD
Pri_B41	PAD5/KWAD5/AN5	Pri_A41	PP0/KWP0/ETRIG0/API_EXTCLK
Pri_B42	PAD6/KWAD6/AN6	Pri_A42	PP1/KWP1/ETRIG1/EXTCLKX2
Pri_B43		Pri_A43	PP2/KWP2/ETRIG2/PWM2
Pri_B44		Pri_A44	PP3/KWP3/ETRIG3/PWM3
Pri_B45		Pri_A45	PP4/KWP4/PWM4
Pri_B46		Pri_A46	PP5/KWP5/PWM5
Pri_B47		Pri_A47	
Pri_B48		Pri_A48	
Pri_B49	**Ground**	Pri_A49	**Ground**
Pri_B50		Pri_A50	
Pri_B51		Pri_A51	
Pri_B52		Pri_A52	
Pri_B53		Pri_A53	
Pri_B54		Pri_A54	
Pri_B55		Pri_A55	
Pri_B56		Pri_A56	
Pri_B57		Pri_A57	
Pri_B58		Pri_A58	
Pri_B59		Pri_A59	
Pri_B60		Pri_A60	PT5/IOC5
Pri_B61		Pri_A61	PT4/IOC4
Pri_B62		Pri_A62	PT3/IOC3
Pri_B63		Pri_A63	
Pri_B64		Pri_A64	
Pri_B65	**Ground**	Pri_A65	**Ground**
Pri_B66		Pri_A66	
Pri_B67		Pri_A67	
Pri_B68		Pri_A68	
Pri_B69		Pri_A69	
Pri_B70		Pri_A70	
Pri_B71		Pri_A71	
Pri_B72		Pri_A72	
Pri_B73		Pri_A73	
Pri_B74		Pri_A74	
Pri_B75		Pri_A75	
Pri_B76		Pri_A76	
Pri_B77		Pri_A77	
Pri_B78		Pri_A78	
Pri_B79		Pri_A79	
Pri_B80		Pri_A80	
Pri_B81	**Ground**	Pri_A81	**Ground**
Pri_B82	**3.3V Power**	Pri_A82	**3.3V Power**

Figure 13: Secondary Edge Connector

Sec_B01	**5.0V Power**	Sec_A01	**5.0V Power**
Sec_B02	**Ground**	Sec_A02	**Ground**
Sec_B03		Sec_A03	
Sec_B04	Elevator Power Sense	Sec_A04	
Sec_B05	**Ground**	Sec_A05	**Ground**
Sec_B06	**Ground**	Sec_A06	**Ground**
Sec_B07	PS1/TXD0	Sec_A07	
Sec_B08		Sec_A08	
Sec_B09	PS2/RXD1	Sec_A09	
Sec_B10	PS3/TXD1	Sec_A10	
Sec_B11	PS4/MISO0	Sec_A11	
Sec_B11A			
Sec_B12		Sec_A12	
Sec_B13		Sec_A13	
Sec_B14		Sec_A14	
Sec_B15		Sec_A15	
Sec_B16		Sec_A16	
Sec_B17		Sec_A17	
Sec_B18		Sec_A18	
Sec_B19		Sec_A19	
Sec_B20		Sec_A20	
Sec_B21		Sec_A21	
Sec_B22		Sec_A22	
Sec_B23		Sec_A23	
Sec_B24		Sec_A24	
Sec_B25		Sec_A25	
Sec_B26	**Ground**	Sec_A26	**Ground**
Sec_B27		Sec_A27	PAD7/KWAD7/AN7
Sec_B28		Sec_A28	VDDA/VRH (NC CT to VDD)
Sec_B29		Sec_A29	VSSA (NC CT to GND)
Sec_B30		Sec_A30	PS0/RXD0
Sec_B31	**Ground**	Sec_A31	**Ground**
Sec_B32		Sec_A32	
Sec_B33		Sec_A33	
Sec_B34		Sec_A34	
Sec_B35		Sec_A35	
Sec_B36	**3.3V Power**	Sec_A36	**3.3V Power**
Sec_B37		Sec_A37	
Sec_B38		Sec_A38	
Sec_B39		Sec_A39	
Sec_B40		Sec_A40	
Sec_B41		Sec_A41	
Sec_B42		Sec_A42	
Sec_B43		Sec_A43	
Sec_B44		Sec_A44	
Sec_B45		Sec_A45	

Sec_B46		Sec_A46	
Sec_B47		Sec_A47	
Sec_B48		Sec_A48	
Sec_B49	**Ground**	Sec_A49	**Ground**
Sec_B50		Sec_A50	
Sec_B51		Sec_A51	
Sec_B52		Sec_A52	
Sec_B53		Sec_A53	
Sec_B54		Sec_A54	
Sec_B55		Sec_A55	
Sec_B56		Sec_A56	
Sec_B57		Sec_A57	
Sec_B58		Sec_A58	
Sec_B59		Sec_A59	
Sec_B60		Sec_A60	
Sec_B61		Sec_A61	
Sec_B62		Sec_A62	
Sec_B63		Sec_A63	
Sec_B64		Sec_A64	
Sec_B65	**Ground**	Sec_A65	**Ground**
Sec_B66		Sec_A66	
Sec_B67		Sec_A67	
Sec_B68		Sec_A68	
Sec_B69		Sec_A69	
Sec_B70		Sec_A70	
Sec_B71		Sec_A71	
Sec_B72		Sec_A72	
Sec_B73		Sec_A73	
Sec_B74		Sec_A74	
Sec_B75		Sec_A75	
Sec_B76		Sec_A76	
Sec_B77		Sec_A77	
Sec_B78		Sec_A78	
Sec_B79		Sec_A79	
Sec_B80		Sec_A80	
Sec_B81	**Ground**	Sec_A81	**Ground**
Sec_B82	**3.3V Power**	Sec_A82	**3.3V Power**