DOC-0559-010, REV A

TWR-PXS20

TOWER Board for Freescale
PXS20 Microcontroller

USER GUIDE

Web Site: www.axman.com
Support: support@axman.com

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TABLES

REVISION

Date	Rev	Comments
September 21, 2011	A	Initial Release

PURPOSE

This document provides design and usage information for the TWR-PXS20 evaluation, development, and reference platform.

The TWR-PXS20 module provides an evaluation system for the Freescale PXS20 embedded microcontroller (MCU) family. This module may be used as a stand-alone development platform or may be used with the Freescale TOWER system. The PXS20 is designed for applications requiring a high Safety Integrity Level (SIL). The on-chip Cross-Triggering Unit (CTU) provides high-end electric motor controls with minimal CPU intervention.

The PXS20 applies 2, e200z4d cores operating in Lock-Step Mode (LS) or Decoupled Parallel Mode (DPM). The device applies Lock Step Redundancy Checking Units at each Sphere of Replication (SOR) output. A programmable fault collection and control unit monitors the integrity status of the device and provides flexible safe state control. Refer to the PXS20 Reference Manual for further details.

REFERENCE DOCUMENTS

Document	Vendor	Location
TWR-PXS20 User Guide	Axiom Manufacturing	www.axman.com/support
TWR-PXS20 Schematic		
PXS20 Reference Manual	Freescale Semiconductor	www.freescale.com
PXS20 Datasheet		
TWRPI Hardware Specification		
TJA1051 High Speed CAN Transceiver	NXP	www.nxp.com
SP485E Half-Duplex RS-485 Transceiver	Exar	www.exar.com
Installation and Operation of the OSBDM	P&E Microcomputer	www.pemicro.com

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the TWR-PXS20 board:

   a) This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may affect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development module utilizes option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that electrically connects 2 terminals

Jumper ON, IN, or installed – jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle – jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

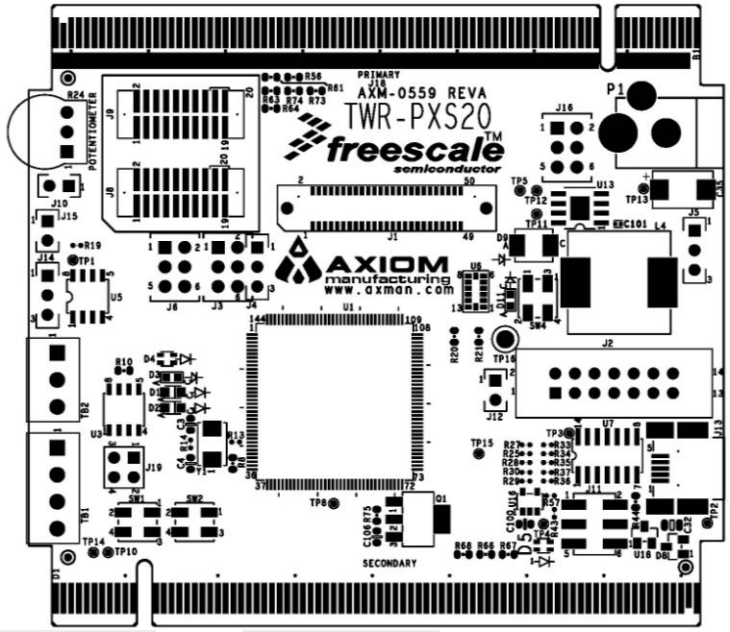
Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Signal names followed by an asterisk (*) denote active-low signals.

FEATURES

The TWR-PXS20 is a demonstration module for the PXS20 embedded processor. The module may be used as a stand-alone development platform or may be used with the Freescale Tower system, a modular development platform which aids in rapid prototyping and tool-reuse. The PXS20 reduces the effort and cost of achieving IEC61508 or comparable Security Integration Level (SIL) certification. An internal Cross-Triggering Unit eases high-end motor control. A programmable fault collection and control unit monitors the integrity status of the device and provides flexible safe state control.

An integrated Open-Source JTAG, software tools, and examples provided with the development board make application development and debug quick and easy. All MCU signals are available on one or both edge connectors.



- PXS20 MCU, 144LQFP
  - 2ea., e200z4d Cores
  - 120MHz internal bus
  - 1 MB Code/Data FLASH
  - 128 KB Internal SRAM
  - 16 Entry MMU
  - Fault Collection and Control Unit (FCCU)
  - 3 ea, SPI Modules
- MMA7455L, 10 bit, Digital Accelerometer
- Integrated Open Source JTAG (OSJTAG)
- 2 ea, debug port headers for external NEXUS or JTAG cable support
- Barrel Connector for External Voltage Input – 5V, ± 5% input only
- On-board +3.3V regulator
- Power input from OSJTAG, Tower System, or barrel connector
- Core Voltage from an on-board SMPS or external header
- Power Input Selection Jumpers
  - +5V Source Selection
  - +3.3V Source Selection
  - +1.2V Source Selection
- Peripherals
  - 3 Push Button Switches, 2 User, 1 Reset
  - 7 LED Indicators, 4 User, 2 OSJTAG, 1 Power
  - 5K ohm POT
  - RS-485 Transceiver w/ terminal block
  - CAN Transceiver w/ 3-pos header
  - TWRPI socket headers for General Purpose TWRPI Module
- Option Jumpers to disconnect User Peripherals
- Connectors
  - 2 ea, 20 pos TWRPI Module Connectors
  - 1 ea, 3 pos Screw-Type Terminal Blocks

- 1 ea, 4 pos Screw-Type Terminal block
- 1 ea, 5 pos USB Connector, Type mini-B
- 1 ea, 50 pos, NEXUS-5001 header
- 1ea, 14 pos JTAG connector

Specifications:
Board Size: 3.53" x 3.18" overall
Power Input: +5V to module barrel connector;

MEMORY MAP

Table 1 below shows a partial memory map highlighting memory locations for board level peripherals applied to the TWR-PXS20. Selected areas shown below are available in both Lock-Step Mode and Decoupled Parallel Mode. Remaining internal MCU peripherals are accessible on either the Primary or Secondary Elevator connectors. Refer to the PXS20 Reference Manual for details and memory location of peripherals and memory areas not shown.

Table 1: Memory Map – Selected

Start Address	Size (KB)	PCTL[1]	Mode	Module Name
0x0000_0000		--	LS/DP	Flash Memory Array Partitions 1 - 4
0x00F0_0000	1		LS/DP	Shadow Flash Block
0x0100_0000	496		LS/DP	Flash Memory Emulation
0x4000_0000	64		DP	SRAM
	128		LS	SRAM
0x5000_0000	64		DP	SRAM[2]
0xFFE0_0000	16	32	LS/DP	A2D Converter 0 (ADC_0)
0xFFE0_4000	16	33	LS/DP	A2D Converter 1 (ADC_1)
0xFFE0_C000	16	35	LS/DP	Cross-Triggering Unit (CTU)
0xFFE4_0000	16	48	LS/DP	LINFlexD_0
0xFFE4_4000	16	49	LS/DP	LINFlexD_1
0xFFE6_C000	16	59	LS/DP	Fault Collection and Control Unit (FCCU)
0xFFF9_0000	16	4	LS/DP	DSPI_0
0xFFFC_0000	16	16	LS/DP	FlexCAN 0 (CAN0)
0xFFFC_4000	16	17	LS/DP	FlexCAN 1 (CAN1)
0xFFFF_C000	16	31	LS/DP	Boot Assist Module (BAM)

[1] Associated Mode Entry Module Peripheral Control Register
[2] This area not accessible by DMA_0

Refer to the PXS20 Reference Manual, available on the Freescale web site for additional details on memory organization and peripheral addressing.

DEVELOPMENT SUPPORT

Application development and debug for the target PXS20 MCU is supported through one of 3 interfaces; a 14 position JTAG connector, a 50 position NEXUS connector or an integrated OSJTAG circuit. The JTAG and NEXUS connectors are applied to support use of external development cables. Pin-out for the JTAG and NEXUS connectors' follows industry standards for NEXUS and IEEE 1149.1 JTAG Test Access Port.

An integrated OSJTAG is applied to the TWR-PXS20 to simplify application development and debug. The OSJTAG provides a standard IEEE 1149.1 Test Access Port (JTAG) interface to allow quick and easy application code development and debug. The OSJTAG can also supply power to the development board. Users connect to the OSJTAG interface using a standard USB cable. The USB specification, however, limits the amount of input current available to the board to 500mA.

CAUTION:

When powering the TWR-PXS20 from the USB bus, do not exceed the 500mA maximum current drain allowed by the USB specification.

Damage to the target board or host PC may result otherwise

OSJTAG Bootloader

The OSJTAG is pre-programmed with a bootloader application allowing field updates of the OSJTAG firmware (FW). The OSJTAG Bootloader is enabled by shorting the terminals of option header J12. The J12 option header is not installed in default configuration. Documentation and utilities for the OSJTAG can be downloaded from the P&E Microcomputer web site at www.pemicro.com.

JTAG Header

A 14 position, IEEE 1149.1 Test Access Port header is applied to support use of an external JTAG debug cable.

NEXUS Header

A 50 position, NEXUS Port header is applied to support use of an external NEXUS debug cable.

SYSTEM POWER

Power to the TWR-PXS20 board may be applied from the Freescale Tower System, through an on-board barrel jack, or through the OSJTAG. The TWR-PXS20 may also source power to the Tower System. The TWR-PXS20 applies several voltage rails; including +5V, +3.3V, and +1.2V. Several option jumpers are applied to facilitate power supply configuration. Table 8 below shows the default setting for each voltage selection header.

CAUTION:

Limit input voltage at the barrel connector, P1, to 5.0V ±5%. Damage the TWR-PXS20 board will result if excessive voltage is applied at this input.

Available power to the TWR-PXS20 module depends on the selected source. Power from the OSJTAG is limited to 2W (+5V @ 500mA) across all voltage rails. Power from the TOWER system is limited to 2W applies to all Tower modules and peripherals. Power from the barrel connector is limited to 10W.

CAUTION:

The barrel connector input does not provide reverse-polarity or transient protection. Ensure input power is conditioned and well defined. Damage to the module may result otherwise.

The +5V rail input selection is made using a 2x3 option header at location J16. This option header selects +5V input from the Tower Elevator, the OSJTAG, or the barrel connector input. The +3.3V rail input selection is made using a 1x3 option header at location J5. Sources include the Tower Elevator or an on-board switching power supply at U13. The +1.2V input rail input selection is generated by the device PMU and an external ballast transistor. No accommodation is made for supplying +1.2V externally.

Pin-out for each power select option header can be found in Table 8 below.

RESET

RESET sources for the TWR-PXS20 include the primary Tower Elevator connector, the OSJTAG, and an on-board push-button switch. A red LED indicates when the RESET line is active. The PXS20 applies both POR and LVD reset circuitry to ensure guaranteed operation during low- voltage conditions.

TIMING

The PXS20 applies a 16 MHz, internal RC oscillator by default out of RESET. An external, 40 MHz crystal oscillator is applied for finer timing control. Maximum bus frequency for this device is 120 MHz.

ACCELEROMETER

The TWR-PXS20 applies a MMA7455L, digital output accelerometer. The MMA7455L applies a serial interface configurable at either I2C or SPI. The accelerometer features signal conditioning, a low-pass filter, temperature compensation and a self-test. Refer to the MMA7455L datasheet for details on use and configuration. Download datasheet, documentation and application notes for the MMA7455L from www.freescale.com.

COMMUNICATIONS

Communications for the TWR-PXS20 module include an RS-485 transceiver and a CAN bus transceiver. A 3 position, screw terminal block supports external connections for the RS-485 channel. A 1x3 header supports external connections for the CAN channel.

RS-485

The TWR-PXS20 board applies an Exar, SP485E, half-duplex, RS-485 transceiver for off-board, serial communications. The transceiver supports communications rates to 10 Mbaud and applies enhanced ESD protection. Separate transmit enable and receive enable inputs support MCU control of communications directions. The RS-485 transceiver connects to the MCU on the LINFlexD_0 channel. Two GPIO outputs provide transmit direction control. An option header at J19 allows both GPIO signals to disconnect from the transceiver. These transceiver inputs are biased MCU to RS-485 transceiver connections are shown in Table 2 below.

Table 2: RS-485 Signal Connections

MCU		RS-485 Transceiver U3		Enable J19	Function
Pin	Signal	Pin	Signal		
V20	LIN0_TXD	4	DI	--	Transmit Data
W20	LIN0_RXD	1	RO	--	Receive Data
D18	GPIO142	3	DE	1 – 2	Transmit Enable, Active High
A20	GPIO144	2	RE*	3 – 4	Receive Enable , Active Low

Shutdown Mode

The applied transceiver applies a Shutdown Mode supporting low-power operation. In Shutdown Mode, quiescent current typically drops to approximately 1 µA. Shutdown Mode is enabled by forcing both DE and RE* to inactive states. The RS-485 transceiver is biased for Shutdown Mode when option jumpers at J19 are removed. A state table for the SP485 transceiver is shown in Table 3 below.

Table 3: RS-485 Transceiver State Table

Transmit State Table						Receive State Table			
Inputs				Outputs		Inputs			Output
RE*	DE	DI	Line Condition	A	B	RE*	DE	A – B	R
X	1	1	No Fault	1	0	0	0	+0.2V	1
X	1	0	No Fault	0	1	0	0	+0.2V	0
X	0	X	X	Z	Z	0	0	Inputs Open	1
X	1	X	No Fault	Z	Z	1	0	X	Z (1)

(1) Shutdown Mode – default mode when J19 jumpers are removed

Refer to the Exar, SP485E for further details on use and capabilities of the applied RS-485 transceiver. The datasheet may be downloaded at www.exar.com.

CAN

The TWR-PXS20 applies an NXP, TJA1051, high-speed CAN transceiver to interface between the FlexCAN_0 controller and the physical, two-wire CAN bus. The transceiver is designed for high-speed applications in the automotive and industrial industries. The transceiver provides differential transmit and receive capability to other CAN protocol controllers. The transceiver supports Silent Mode, which disables the transmitter, releasing the CAN bus. The CAN transceiver is configured for NORMAL operation by default. A test point is applied on the transceiver S input to enable SILENT mode. Table 4 below shows the different operation modes for the on-board CAN transceiver.

The TJA1051, CAN transceiver connects to the MCU on FLEXCAN_0.

Table 4: CAN Transceiver Operating Modes

MODE	Inputs		Outputs	
	S	TXD	CAN Driver	RXD
Normal	LOW	LOW	Dominate	Active (1)
	LOW	HIGH	Recessive	Active (1)
Silent	High	X	Recessive	Active (1)

(1) LOW if CAN bus is dominate, HIGH if CAN bus is recessive

Refer to the TJA1051 datasheet for further details on configuration and use of the CAN transceiver. The datasheet may be downloaded from www.nxp.com.

CAN Select Option Header

The FlexCAN_0 module is routed to CAN transceiver and to the secondary Tower Elevator connector. A 2x3 pin header at J6 routes the FlexCAN_0 module signals as needed. Table 8 below shows default settings for all option jumpers.

CAN Termination Option Header

An option header at J15 applies 120 ohm termination to input physical CAN bus. Removing the jumper, disconnects CAN termination. Installing the jumper connects a single, 120 ohm resistor across the input CAN bus signal lines. Table 8 below shows default settings for all option jumpers.

TWRPI SOCKET

The TWR-PXS20 applies a General Purpose Tower Plug-In (TWRPI) socket. The TWRPI socket consists of 2, keyed socket headers arranged to accept the majority of TWRPI modules. Refer to the Tower Plug-in (TWRPI) Specification for the Freescale Tower System, TWRPI HW Guide, for details. The TWRPI HW Guide is available at www.freescale.com.

FAULT CORRECTION & CONTROL UNIT

The PXS20 applies a Fault Collection and Control Unit (FCCU). The FCCU provides a programmable, redundant, hardware channel to collect errors and allow deterministic device behavior when a fault is detected. No CPU intervention is required for collection and control operation.

The FCCU generates 2 external signals, FCCU_F[1:0]. The TWR-PXS20 routes both signals to an XOR gate which drives a red, active low LED at D3. Pin behavior for both FCCU_Fx pins may be configured under user control; however, on the TWR-PXS20, pin behavior should be configured as shown in Table 5 below.

Table 5: FCCU Output Configuration

Condition	State	LED – RED
Normal	FCCU_F[1:0] toggle in opposite state	D3
Fault	FCCU_F[1:0] toggle in same state	D3

USER PERIPHERALS

User I/O includes 1 potentiometer, 4 push button switches, and 4 green LEDs for user I/O. The sections below describe the functionality of each user peripheral.

Potentiometer

The TWR-PXS20 applies a single-turn, 5K, ohm potentiometer (POT) to simulate analog input. The POT is connected to an analog input on the target MCU. An option jumper at J10 connects the POT to the MCU. Table 8 below shows the USER jumper settings.

User LED's

The TWR-PXS20 applies 4 LEDs for output indication. Installed LEDs include; 2 green LEDS, and 1 dual, red/green LED. Each LED is configured for active-low operation. A series, current-limit resistor prevents excessive diode current. Each LED is connected to a GPIO output as shown in Table 6 below.

Table 6: User LED Connections

Signal Name	LED	LED Color
GPIO106	D1	Green
GPIO 83	D2	Green
GPIO54	D4-2	Red
GPIO107	D4-4	Green

Pushbutton Switches

The TWR-PXS20 applies 2 push-button switches (PBSW) connected to IRQ* inputs. Each push-button switch is configured for active-low operation with an external pull-up applied for deterministic behavior. Both PBSWs are connected to IRQ* input that may also be configured for GPIO operation. Table 7 below shows the push button switch connections.

Table 7: Push Button Switch Connections

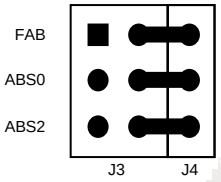
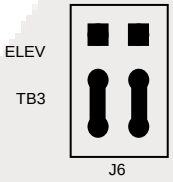
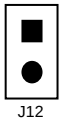
PB Switch	MCU Signal	Function
SW1	DSPI2_SOUT (EIRQ11*)	IRQ* or GPIO input
SW2	DSPI2_SIN (EIRQ12*)	IRQ* or GPIO Input
SW4	RESET_B	Reset Input

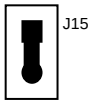
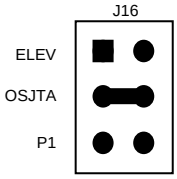
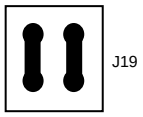
OPTION JUMPER SETTINGS

The table below shows default setting for each of the option header on the TWR-PXS20 board. The text adjacent to each image below does not appear on the board. This text is added for clarity to the table. Refer to the PXS20 Reference Manual and TWR-PXS20 Schematic for further details on use and configuration of each jumper.

The square pin in each image below indicates pin 1.

Table 8: Option Jumper Settings

Option Jumper	Default Setting	Comments
J3 / J4		Alternate Boot Mode Select: Use to configure boot mode. Single chip mode setting shown.
J5		3V3_SYS Select: Select source for +3.3V rail. On-board regulators setting shown.
J6		CAN Select: Select CAN output destination. TB3 setting shown.
J10		POT Enable Enables POT connection to target MCU ADC0_AN8 input.
J12		OSJTAG Bootloader Enable Enables OSJTAG Bootloader. This header is not populated by default.

J15		CAN Termination Enable CAN termination by default.
J16		Input Power Select Select OSJTAG input power by default.
J19		CAN Control Signal Enable Connects CAN transceiver flow control signals to target MCU.

CONNECTORS

The following table shows the pin-out for the various connector headers used on the TWR-PXS20 board.

Table 9: Connector Pin-Out

J14 – CAN BUS Connector

CANH	1
GND	2
CANL	3

Physical CAN bus input connector. This is a 3-pos, .1" center header.

TB1 – RS-485 BUS Terminal Block

A	1
B	2
GND	3

Physical RS-485 bus input connector. 3-pos, 3.55mm centers, screw-type terminal block

TB2 – Analog Input Terminal Block

+5V	1
ADC1_AN5	2
ACD2_AN7	3
GND	4

Analog input connector. This is a 4-pos, 3.5mm terminal block.

J1 – NEXUS Connector

Signal			Signal	Description
MSEO0	1	2	TCK	SAMTEC, ERF8 connector applied to support high-speed NEXUS debug cables. Connector complies with NEXUS5001 standards.
MSEO1	3	4	TMS	
GND	5	6	TDI	
MDO0	7	8	TDO	
MDO1	9	10	TCK	This connector allows application development and debug for target MCU.
GND	11	12	JCOMP	
MDO2	13	14		
MDO3	15	16	EVTI	
GND	17	18	EVTO	
MCKO	19	20	RESET_B	
	21	22		
GND	23	24	GND	
	25	26		
	27	28		
GND	29	30	GND	
	31	32		
	33	34		
GND	35	36	GND	
	37	38		
	39	40		
GND	41	42	GND	
	43	44		
	45	46		
GND	47	48	GND	
	49	50		

J2 – JTAG Connector

TDI	1	2	GND	IEEE 1149.1 Test Access Port header applied to support JTAG debug cables. This is a 14-pos, .1” center header
TDO	3	4	GND	
TCK	5	6	GND	
	7	8		
RESET_B	9	10	TMS	This connector allows application development and debug for target MCU.
+3.3V	11	12	GND	
	13	14	JCOMP	

J11 – OSJTAG BDM Connector

JM60_BKGD	1	2	GND	BDM connector for integrated OSJTAG. Supports OSJTAG application development and debug. This is a 6-pos, .1” center header
	3	4	JM60_RESET_B	
	5	6	JM50_VDD	

J13 – OSJTAG Connector

A standard USB, type mini-B connector

EDGE CONNECTOR PIN-OUT

The TWR-S12GN board connects to the Freescale Tower System using the 2 PCIe Edge Connectors. Following the PCIe specification, the Bx signals are located on the top of the board and the Ax signals are located on bottom. Pin B1 for the primary and secondary connectors are at opposite corners of the board. Table 10 and Table 11 below show the pin-out the primary and secondary edge connectors. Pin positions with no signal name shown are not connected.

Table 10: Primary Edge Connector

Pri_B01	**5.0V Power**	Pri_A01	**5.0V Power**
Pri_B02	**Ground**	Pri_A02	**Ground**
Pri_B03		Pri_A03	
Pri_B04	Elevator Power Sense	Pri_A04	
Pri_B05	**Ground**	Pri_A05	**Ground**
Pri_B06	**Ground**	Pri_A06	**Ground**
Pri_B07	DSPI1_SCK	Pri_A07	
Pri_B08	DSPI1_CS1*	Pri_A08	
Pri_B09	DSPI1_CS0*	Pri_A09	GPIO53
Pri_B10	DSPI1_SOUT	Pri_A10	GPIO51
Pri_B11	DSPI1_SIN	Pri_A11	GPIO93
KEY			
Pri_B12		Pri_A12	
Pri_B13		Pri_A13	
Pri_B14		Pri_A14	
Pri_B15		Pri_A15	
Pri_B16		Pri_A16	
Pri_B17		Pri_A17	
Pri_B18		Pri_A18	
Pri_B19		Pri_A19	
Pri_B20		Pri_A20	
Pri_B21	GPIO42	Pri_A21	
Pri_B22	GPIO49	Pri_A22	
Pri_B23	GPIO50	Pri_A23	
Pri_B24		Pri_A24	
Pri_B25		Pri_A25	
Pri_B26	**Ground**	Pri_A26	**Ground**
Pri_B27	ADC0_AN7	Pri_A27	ADC0_AN3
Pri_B28	ADC0_AN6	Pri_A28	ADC0_AN2
Pri_B29	ADC0_AN5	Pri_A29	ADC0_AN1
Pri_B30	ADC0_AN4	Pri_A30	ADC0_AN0
Pri_B31	**Ground**	Pri_A31	**Ground**
Pri_B32		Pri_A32	SWG
Pri_B33	ETIMER0_ETC5	Pri_A33	ETIMER0_ETC3
Pri_B34	ETIMER0_ETC4	Pri_A34	ETIMER0_ETC2
Pri_B35	GPIO73	Pri_A35	GPIO74

Pri_B36	**3.3V Power**	Pri_A36	**3.3V Power**
Pri_B37	FLEXPWM0_B3	Pri_A37	FLEXPWM0_B1
Pri_B38	FLEXPWM0_A3	Pri_A38	FLEXPWM0_A1
Pri_B39	FLEXPWM0_B2	Pri_A39	FLEXPWM0_B0
Pri_B40	FLEXPWM0_A2	Pri_A40	FLEXPWM0_A0
Pri_B41	FLEXCAN1_RXD	Pri_A41	LIN0_RXD
Pri_B42	FLEXCAN1_TXD	Pri_A42	LIN0_TXD
Pri_B43		Pri_A43	LIN1_RXD
Pri_B44	DSPI0_SIN	Pri_A44	LIN1_TXD
Pri_B45	DSPI0_SOUT	Pri_A45	
Pri_B46	DSPI0_CS0*	Pri_A46	VDDA
Pri_B47	DSPI0_CS1*	Pri_A47	CAN0_RXD
Pri_B48	DSPI0_SCK	Pri_A48	CAN0_TXD
Pri_B49	**Ground**	Pri_A49	**Ground**
Pri_B50		Pri_A50	GPIO25
Pri_B51		Pri_A51	GPIO26
Pri_B52	GPIO52	Pri_A52	GPIO27
Pri_B53		Pri_A53	GPIO28
Pri_B54		Pri_A54	
Pri_B55	FLEXPWM0_FAULT0	Pri_A55	
Pri_B56	FLEXPWM0_FAULT0	Pri_A56	
Pri_B57	DSPI2_SCK	Pri_A57	
Pri_B58	DSPI2_SCK	Pri_A58	
Pri_B59	DSPI2_CS0*	Pri_A59	
Pri_B60	DSPI2_CS0*	Pri_A60	
Pri_B61	IRQ25*	Pri_A61	
Pri_B62	NMI*	Pri_A62	
Pri_B63		Pri_A63	RESET_B
Pri_B64		Pri_A64	CLK_OUT0
Pri_B65	**Ground**	Pri_A65	**Ground**
Pri_B66		Pri_A66	
Pri_B67		Pri_A67	
Pri_B68		Pri_A68	
Pri_B69		Pri_A69	
Pri_B70		Pri_A70	
Pri_B71		Pri_A71	
Pri_B72		Pri_A72	
Pri_B73		Pri_A73	
Pri_B74		Pri_A74	
Pri_B75		Pri_A75	
Pri_B76		Pri_A76	
Pri_B77		Pri_A77	
Pri_B78		Pri_A78	
Pri_B79		Pri_A79	
Pri_B80		Pri_A80	
Pri_B81	**Ground**	Pri_A81	**Ground**
Pri_B82	**3.3V Power**	Pri_A82	**3.3V Power**

Table 11: Secondary Edge Connector

Sec_B01	**5.0V Power**	Sec_A01	**5.0V Power**
Sec_B02	**Ground**	Sec_A02	**Ground**
Sec_B03		Sec_A03	
Sec_B04	Elevator Power Sense	Sec_A04	
Sec_B05	**Ground**	Sec_A05	**Ground**
Sec_B06	**Ground**	Sec_A06	**Ground**
Sec_B07		Sec_A07	
Sec_B08		Sec_A08	
Sec_B09		Sec_A09	
Sec_B10		Sec_A10	
Sec_B11		Sec_A11	
KEY			
Sec_B12		Sec_A12	
Sec_B13		Sec_A13	
Sec_B14		Sec_A14	
Sec_B15		Sec_A15	
Sec_B16	GPIO76	Sec_A16	
Sec_B17		Sec_A17	
Sec_B18		Sec_A18	
Sec_B19		Sec_A19	
Sec_B20		Sec_A20	
Sec_B21		Sec_A21	
Sec_B22		Sec_A22	
Sec_B23		Sec_A23	
Sec_B24		Sec_A24	
Sec_B25		Sec_A25	
Sec_B26	**Ground**	Sec_A26	**Ground**
Sec_B27		Sec_A27	ADC1_AN3
Sec_B28		Sec_A28	ADC1_AN2
Sec_B29	ADC1_AN5	Sec_A29	ADC1_AN1
Sec_B30	ADC1_AN4	Sec_A30	ADC1_AN0
Sec_B31	**Ground**	Sec_A31	**Ground**
Sec_B32		Sec_A32	
Sec_B33	ETIMER1_ETC4	Sec_A33	ETIMER1_ETC1
Sec_B34	ETIMER1_ETC2	Sec_A34	ETIMER1_ETC0
Sec_B35		Sec_A35	
Sec_B36	**3.3V Power**	Sec_A36	**3.3V Power**
Sec_B37		Sec_A37	
Sec_B38		Sec_A38	
Sec_B39		Sec_A39	
Sec_B40		Sec_A40	
Sec_B41		Sec_A41	
Sec_B42		Sec_A42	
Sec_B43		Sec_A43	
Sec_B44		Sec_A44	
Sec_B45		Sec_A45	

Sec_B46		Sec_A46	
Sec_B47		Sec_A47	
Sec_B48		Sec_A48	
Sec_B49	**Ground**	Sec_A49	**Ground**
Sec_B50		Sec_A50	
Sec_B51		Sec_A51	
Sec_B52		Sec_A52	
Sec_B53		Sec_A53	
Sec_B54		Sec_A54	
Sec_B55		Sec_A55	
Sec_B56		Sec_A56	
Sec_B57	ETIMER1_ETC5	Sec_A57	
Sec_B58	ETIMER1_ETC5	Sec_A58	
Sec_B59	ETIMER0_ETC1	Sec_A59	
Sec_B60	ETIMER0_ETC1	Sec_A60	
Sec_B61	ETIMER0_ETC0	Sec_A61	
Sec_B62	ETIMER0_ETC0	Sec_A62	
Sec_B63		Sec_A63	
Sec_B64		Sec_A64	
Sec_B65	**Ground**	Sec_A65	**Ground**
Sec_B66		Sec_A66	
Sec_B67		Sec_A67	
Sec_B68		Sec_A68	
Sec_B69		Sec_A69	
Sec_B70		Sec_A70	
Sec_B71		Sec_A71	
Sec_B72		Sec_A72	
Sec_B73		Sec_A73	
Sec_B74		Sec_A74	
Sec_B75		Sec_A75	
Sec_B76		Sec_A76	
Sec_B77		Sec_A77	
Sec_B78		Sec_A78	
Sec_B79		Sec_A79	
Sec_B80		Sec_A80	
Sec_B81	**Ground**	Sec_A81	**Ground**
Sec_B82	**3.3V Power**	Sec_A82	**3.3V Power**