TWR-ADCDAC-AX

Analog Module for Freescale TOWER System

HARDWARE USER GUIDE

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Revision

Date	Rev	Comments
May 8, 2013	A	Initial Release

Cautionary Notes

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information for the TWR-ADCDAC-AX board:

   a) This product has not been tested for compliance to CE and FCC requirements. The user has responsibility to ensure this product neither adversely affects nearby electronic equipment nor suffers adverse effects from nearby electronic equipment.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may affect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

Terminology

This development module utilizes option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

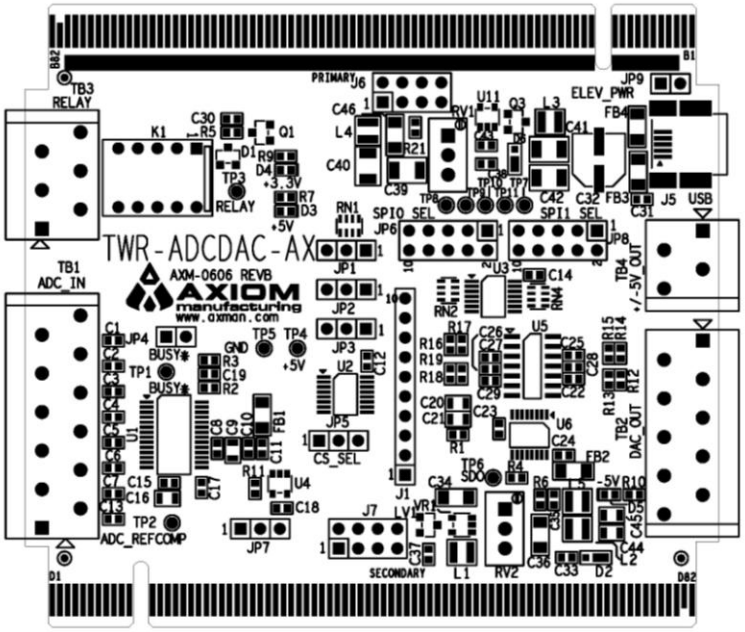
Signal names followed by an asterisk (*) denote active-low signals.

FEATURES

The TWR-ADCDAC-AX is a Tower Peripheral Module designed for use with the Freescale Tower System. This board features 1 analog-to-digital converter (ADC) and 1 digital-to-analog converter (DAC) from Linear Technology. A user-selectable DAC reference voltage input selects between 1.22 mV per step and 1.0 mV per step output. Two SPI input channels allow any Tower Controller Module to interface to the TWR-ADCDAC-AX.

While designed specifically for use with the TWR-S12G128, the TWR-ADCDAC-AX board will function normally with any Tower Module which supports SPI communications on TOWER Elevator SPI0 or SPI1 ports.

Module Features:



1 ea. 8-Ch, 12-bit Analog-to-Digital Converter
- LTC1857CG
- Software Programmable Input Ranges:
  - 0–5 V, 0–10V
  - ±5V, ±10V
  - Single-Ended or Differential
- On-Chip Reference Voltage
- Optional External Reference Voltage at TP2
- ± 25 VDC Input Protection
- BUSY* Signal Output available on GPIO

- 1 ea., 8-Ch, 12-bit Digital-to-Analog Converter
  - LTC2620CGN
  - High Rail-to-Rail Output Drive (± 15mA, Min)
  - 8-Ch Uni-Polar and 4-Ch Bi-Polar Outputs
    - Uni-Polar range from 0V to +5V
    - Bipolar range from -5V to +5V
  - Low Input Offset (V_{OS}), Precision Amplifier for Bipolar Outputs
  - Selectable VREF Input
    - +5V or +4.096V
    - +5V REF input provides 1.22 mV per step output
    - +4.096V REF input provides 1.0mV per step output
- On-Board analog +5VA and -5V voltage supplied for use with ADC and DAC
  - POT on each supply output allows fine-tuning each supply separately

- Spring Activated Terminal Block Input and Output Connections
- PCB Footprint Relay with Terminal Block Connector (optional and not populated by default)
  - 2-Ch, NO & NC connections available
  - Transistor-coupled drive control
  - Industry Standard Footprint
  - Through-hole Relay and Terminal Block for easy installation
- Optional Power input from USB connector for high-power applications
- Dual PCI edge connectors interface to Tower Controller Module

Specifications:
Board Size Tower Module Form Factor, 3.54 x 3.17 IN
Voltage Input: 5.5VDC

NOTE:

All signal references in this document assume the use of the TWR-S12G128 MCU story module. It falls to the user to ensure proper signal assignment when using an alternate MCU story board.

CAUTION:

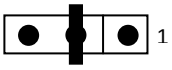
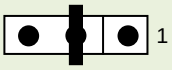
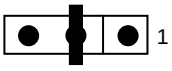
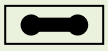
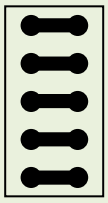
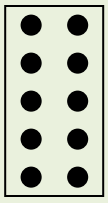
Use care when adjusting potentiometers at RV1 and RV2. These POTs allow fine-tuning the +5_VA and -5V voltage levels to account for component drift. One or both POTs can adjust voltage levels outside of the safe operating range causing damage to the board.

Damage caused by improper adjustment of RV1 and/or RV2 will not be covered under warranty

OPTION HEADERS

The TWR-ADCDAC-AX makes use of option configuration headers. Table 1 below shows default shunt settings, which should support the majority of uses.

Table 1: Default Option Configuration

Option	Name	Ref	Default	Configuration
		JP1	OFF	Option headers JP1, JP2, and JP3 are used to manually set Chip-Select address to the board.
		JP2	OFF	
		JP3	OFF	
	BUSY*	JP4	ON	Connects BUSY* output from ADC to PP7/KWP7.
	CS_SEL	JP5	1 – 2	Selects SPI_CS0 or SPI_CS1when addressing TWR-ADCDAC-AX board.
	SPI0_SEL	JP6	All ON	Connects to MC9S12G128 SPI0 Signals.
		JP7	2 – 3	Selects VREF input to DAC and Bipolar output. 1 – 2: Applies +4.096 providing 1.0mV per step. 2 – 3: Applies +5_VA providing 1.22mV per step.
	SPI1_SEL	JP8	All OFF	Connects to MC9S12G128 SPI1 Signals
	ELEV_PWR	JP9	ON	ON: TWR-ELEV powers board OFF: USB connector powers board

POWER

Users may configure the TWR-ADCDAC-AX board to draw power from the TWR-ELEV or from the on-board USB connector. The USB connector is provided for use in high-power applications. Option jumper at JP9 connects the TWR-ADCDAC-AX power input to the TWR-ELEV by default. When using the USB power input, remove the option shunt at JP9.

This board draws digital power directly from the TWR-ELEV. Two switching power supplies supply analog +5 and -5 voltage levels. Each analog supply includes a potentiometer (POT) to allow fine-tuning of each analog voltage level separately.

Each voltage level applies a single, red LED to indicate its energized state.

Analog Voltage Power Supplies

The TWR-ADCDAC-AX applies a voltage boost circuit to create the +5_VA voltage level. The boost circuit creates a stable, low-ripple output. Additional output filtering further reduces output ripple ensuring a stable voltage level for use during conversion.

An inverting circuit creates a stable, low-ripple output -5V voltage level supporting bipolar output. As with the +5_VA circuit, a POT allows fine-tuning the -5V output and a low-pass, LC filter, circuit further reduces any output ripple. The -5V circuit incorporates a 150ms turn-on delay allowing input power to stabilize.

CAUTION:

Use care when adjusting potentiometers at RV1 and RV2. These POTs allow fine-tuning the +5_VA and -5V voltage levels. POT adjustment allows both voltage levels to increase beyond the safe operating range causing damage to the board.

Damage caused by improper adjustment of RV1 and/or RV2 will not be covered under warranty

COMMUNICATIONS

The TWR-ADCDAC-AX connects to the 9S12G128 MCU through a Serial Peripheral Interface (SPI) on the Primary Elevator. By default, the TWR-ADCDAC-AX is configured to use SPI channel 0 (SPI0), which connects to SPI2 on the 9S12G128 MCU. See Table 2 below for SPI channel signal map relating to the TWR-ADCDAC-AX board. Use of SPI0 requires all option shunts at option header JP6 be ON.

Table 2: SPI Signal Mapping

9S12G128 SPI Channel	9S12G128 Signal	Primary Elevator Signal Name	Connector Pin Number	TWR-ADCDAC-AX Signal Name	Option Header	Position
SPI0	SCK0	SPI1_CLK	B7	SPI1_CLK	JP8	1 – 2
	N/C	SPI1_CS1	B8	SPI1_CS1		7 – 8
	SS0	SPI1_CS0	B9	SPI1_CS0		5 – 6
	MOSI0	SPI1_MOSI	B10	SPI1_MOSI		3 – 4
	MISO0	SPI1_MISO	B11	SPI1_MISO		9 - 10
SPI2	MISO2	SPI0_MISO	B44	SPI0_MISO	JP6	9 – 10
	MOSI2	SPI0_MOSI	B45	SPI0_MOSI		1 – 2
	SS2	SPI0_CS0	B46	SPI0_CS0		7 – 8
	N/C	SPI0_CS1	B47	SPI0_CS1		5 – 6
	SCK2	SPI0_CLK	B48	SPI0_CLK		3 - 4

NOTE: SPI1 does not connect to the TWR-ADCDAC-AX board. S1 signal connections in the table above supports alternate MCU story modules.

MEMORY MAP

The TWR-ADCDAC-AX board provides access to 8 separate chip-selects, CS0* to CS7*. A 3-to-8 multiplexer (MUX) generates each, active low, chip select (CS*). The MUX actively drives unused CS outputs high. When using the 9S12G128, addressing to the MUX originates from Port D signals, PD3 through PD3. SPI2 Slave Select (PJ7/SS2) enables the MUX output. Option headers at JP1, JP2, and JP3 allow the user to configure default CS output if needed.

Active CS generation is recommended. The TWR-ADCDAC-AX board applies CS5* and CS7* exclusively to the DAC and ADC respectively. The user has access to remaining CS outputs at header J1.

Table 3: Chip-Select Addresses

PD[5:3]	Port D	PJ7 / SS2	Chip Select	Access
xxx	xxxx xxxx	1	Disabled	None
000	xx00 0xxx	0	U_CS0	J1-9
001	xx00 1xxx	0	U_CS1	J1-8
010	xx01 0xxx	0	SPI_CS2	J1-7
011	xx01 1xxx	0	SPI_CS3	J1-5
100	xx10 0xxx	0	SPI_CS4	J1-4
101	xx10 1xxx	0	SPI_CS5	DAC
110	xx11 0xxx	0	SPI_CS6	J1-2
111	xx11 1xxx	0	SPI_CS7	ADC

ANALOG TO DIGITAL CONVERTER

The TWR-ADCDAC-AX applies a Linear Technologies, LTC1857, Analog-to-Digital Converter (ADC). The LTC1857 is an 8 channel, 12 bit ADC, 100 ksps device. This ADC supports software selectable input ranges of 0-5V, 0-10V, ±5V, and ±10V. The LTC1857 also supports single-ended inputs, differential inputs, or both. The BUSY* output from the ADC is connected to a GPIO signal on the controlling MCU.

Reading and writing to the ADC is accomplished using the SPI port on the controlling MCU. Default configuration connects the ADC to SPI2 on the 9S12G128.

Proper use of the LTC1857 ADC requires the user to supply a common reference (COM) to the device. This may come from the analog input or may be connected directly to the GND connection on TB1. Refer to the LTC1857 Datasheet for details on use and configuration of this device.

DIGITAL TO ANALOG CONVERTER

The TWR-ADCDAC-AX applies a Linear Technologies, LTC2620, Digital-to-Analog Converter (DAC). The LTC2620 is an 8-channel, 12-bit DAC with rail to rail outputs. A power-on reset circuit (POR) incorporated in the LTC2620 ensures outputs remain at zero-scale until a valid write occurs. The TWR-ADCDAC-AX does not allow read-back from the LTC2620.

Refer to the LTC2620 Datasheet for details on use and configuration of this device.

ANALOG HEADER

The TWR-ADCDAC-AX applies 2 each headers for access to Analog-to-Digital Converters on the 9S12G128 MCU. The 9S12G128 module applies a 16-chl, 10-bit ADC configurable for either 8- or 10-bit output. Refer to the MC9S12G Family Reference Manual for details on the 9S12G128 ADC use and configuration.

Depending on the story module connected, these signals may connect to GPIO signal on the MCU, other signal types on the MCU, or may be No Connects. Please refer to the target MCU Datasheet for details on use and configuration.

RELAY

The TWR-ADCDAC-AX applies an industry standard TQ2-5V relay. The TW2-5V is a non-latching, 2 Form-C relay. The latching coil is transistor coupled to the controlling MCU while a flyback diode quickly dissipates any latching coil charge when no longer driven. The MCU controls the relay behavior through an active-high signal connected to port PD6 on the 9S12G128.

Default configuration has the coupling transistor and flyback diode installed, while the TQ2-5V relay and associated terminal block are not installed.

EDGE CONNECTOR PINOUT

The TWR-ADCADC-AX board connects to the Freescale TOWER System using the 2 PCI Edge Connectors. Following the PCI specification, the Bx signals are located on the top of the board and the Ax signals are located on bottom. Pin B1 for the primary and secondary connectors are at opposite corners of the board. The figures below show the pin-out of each edge connector with 9S12G128 signal in parenthesis. Pin positions with no signal name shown are not connected.

Signal names shown connect to the 9S12G128 MCU. Use of a different MCU board may not support connections as shown. The user has responsibility to ensure appropriate connections when using a different MCU board

Table 4: Primary Edge Connector – J1

Signal Name Top	Pin Number		Signal Name Bottom
	B01	A01	
Ground	B02	A02	**Ground**
	B03	A03	
	B04	A04	
Ground	B05	A05	**Ground**
Ground	B06	A06	**Ground**
SPI1_CLK (PS6/SCK0)	B07	A07	SCL0 (not connected)
SPI1_CS1 (NC)	B08	A08	SDA0 (not connected)
SPI1_CS0 (PS7/SS0)	B09	A09	GPIO9 (PD3)
SPI1_MOSI (PS5/MOSI0)	B10	A10	GPIO8 (PD4)
SPI1_MISO (PS4/MISO0)	B11	A11	GPIO7 (PD5)
	KEY	KEY	
	B12	A12	
	B13	A13	
	B14	A14	
	B15	A15	
	B16	A16	
	B17	A17	
	B18	A18	
	B19	A19	
	B20	A20	
GPIO1 (PD6)	B21	A21	
	B22	A22	
	B23	A23	
	B24	A24	
	B25	A25	
Ground	B26	A26	**Ground**
AD7 (PAD7/AN7)	B27	A27	AD3 (PAD3/AN3)
AD6 (PAD6/AN6)	B28	A28	AD2 (PAD2/AN2)
AD5 (PAD5/AN5)	B29	A29	AD1 (PAD1/AN1)
AD4 (PAD4/AN4)	B30	A30	AD0 (PAD0/AN0)
Ground	B31	A31	**Ground**
	B32	A32	

Signal Name Top	Pin Number		Signal Name Bottom
	B33	A33	
	B34	A34	
	B35	A35	
	B36	A36	
BUSY* (	B37	A37	
	B38	A38	
	B39	A39	
	B40	A40	
	B41	A41	
	B42	A42	
	B43	A43	
SPI0_MIS0 (PJ4/MISO2)	B44	A44	
SPI0_MOSI (PJ5/MOSI2)	B45	A45	
SPI0_CS0 (PJ7/ SS2	B46	A46	
SPI0_CS1 (NC)	B47	A47	
SPI0_CLK(PJ6/SCK2)	B48	A48	
Ground	B49	A49	**Ground**
	B50	A50	
	B51	A51	
	B52	A52	
	B53	A53	
	B54	A54	
	B55	A55	
	B56	A56	
	B57	A57	
	B58	A58	
	B59	A59	
	B60	A60	
	B61	A61	
	B62	A62	
	B63	A63	
	B64	A64	
Ground	B65	A65	**Ground**
	B66	A66	
	B67	A67	
	B68	A68	
	B69	A69	
	B70	A70	
	B71	A71	
	B72	A72	
	B73	A73	
	B74	A74	
	B75	A75	
	B76	A76	
	B77	A77	
	B78	A78	
	B79	A79	
	B80	A80	
Ground	B81	A81	**Ground**
	B82	A82	

Table 5: Secondary Edge Connector – J2

Signal Name Top	Pin Number		Signal Name Bottom
	B01	A01	
Ground	B02	A02	**Ground**
	B03	A03	
	B04	A04	
Ground	B05	A05	**Ground**
Ground	B06	A06	**Ground**
	B07	A07	
	B08	A08	
	B09	A09	
	B10	A10	
	B11	A11	
	KEY	KEY	
	B12	A12	
	B13	A13	
	B14	A14	
	B15	A15	
	B16	A16	
	B17	A17	
	B18	A18	
	B19	A19	
	B20	A20	
	B21	A21	
	B22	A22	
	B23	A23	
	B24	A24	
	B25	A25	
Ground	B26	A26	**Ground**
	B27	A27	AD11 (PAD11/AN11)
	B28	A28	AD10 (PAD10/AN10)
AD13 (PAD13/AN13)	B29	A29	AD9 (PAD9/AN9)
AD12 (PAD12/AN12)	B30	A30	AD8 (PAD8/AN8
Ground	B31	A31	**Ground**
	B32	A32	
	B33	A33	
	B34	A34	
	B35	A35	
	B36	A36	
	B37	A37	
	B38	A38	
	B39	A39	
	B40	A40	
	B41	A41	
	B42	A42	
	B43	A43	
	B44	A44	
	B45	A45	
	B46	A46	
	B47	A47	
	B48	A48	
Ground	B49	A49	**Ground**

Signal Name Top	Pin Number		Signal Name Bottom
	B50	A50	AD14 (PAD14/AN14)
	B51	A51	AD15 (PAD15/AN15)
	B52	A52	
	B53	A53	
	B54	A54	
	B55	A55	
	B56	A56	
	B57	A57	
	B58	A58	
	B59	A59	
	B60	A60	
	B61	A61	
	B62	A62	
	B63	A63	
	B64	A64	
Ground	B65	A65	**Ground**
	B66	A66	
	B67	A67	
	B68	A68	
	B69	A69	
	B70	A70	
	B71	A71	
	B72	A72	
	B73	A73	
	B74	A74	
	B75	A75	
	B76	A76	
	B77	A77	
	B78	A78	
	B79	A79	
	B80	A80	
Ground	B81	A81	**Ground**
	B82	A82	

APPENDIX A

The illustration below shows the ADC input connections and DAC output connections for the TWR-ADCDAC-AX board.