MPC567XEVBMB

Evaluation Base Board Hardware User Guide

Supports
MPC5674ADAT324, MPC567XADAT416,
& MPC567XADAT516 Daughter Boards

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FIGURES

REVISION

Date	Rev	Comments
November 3, 2008	A	Initial Release.
May 18, 2009	B	Update Flex-Ray Connector diagram. Reordered CONFIG_SW numbering
October 12, 2009	C	Corrected alpha revision in document. Updated figure numbers and page numbers
January 11, 2011	D	Added support for MPC5676R MCU
March 16, 2011	E	Corrected title page and table of contents
July 11, 2012	F	Correct Header reference designators in Fig 20 & 21

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be applied whenever handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing reserves the right to make changes without further notice to any products to improve reliability, function or design. Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the MPC567XEVBMB board:

   a) This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may affect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Signal names followed by an asterisk (*) denote active-low signals.

OVERVIEW

The MPC567XEVBMB (EVBMB) provides baseboard functionality for a line of Freescale PowerPC microcontrollers including the MPC5674F and MPC5676R. Several daughter cards (DC) support both MCU's in different package configurations. Daughter Card support includes the MPC5674ADAT324 for the 324 BGA package, the MPC567XADAT416 for the 416 BGA package, and the MPC567XADAT516 for the 516 BGA package. The daughter card mates to the EVBMB via 4, low profile, stack headers. This document details the hardware configuration for the EVBMB. Microcontrollers supported by the

EVBMB CONFIGURATION

CONFIG Switch

The CONFIG switch sets reset configuration options for the target MCU. Switch position 1 enables configuration options. The OFF position applies a low input signal to the MCU. The ON position applies a high signal to the MCU.

Figure 1: CONFIG Switch – SW4

POS	SIGNAL	DEFAULT
1	CONFIG enable	ON
2	BOOTCFG0	ON
3	BOOTCFG1	OFF
4	PLLCFG0	ON
5	PLLCFG1	OFF
6	PLLCFG2	ON
7	WKPCFG	ON
8	Not connected	NA

NOTE: Refer to Freescale MPC5674F or MPC5676R Documentation for detail on setting configuration options.

POWER SUPPLY

The MC33730 APSIC provides primary power to the EVBMB. The APSIC energizes the +5V and +3.3V voltage rails directly. A separate LDO voltage regulator is used to energize the VDD voltage rail to the daughter card. Green LED indicators are provided to show the state of each voltage rail individually.

Power supply reset input signals are connected to the target MCU RESET* signal through cut-traces S1 – S3. Normally open option pads at S0 allow the EVBMB RESET* signal to be applied to the APSIC RSTKAM* input. Simply short option pads using a 0 ohm resistor to enable this function.

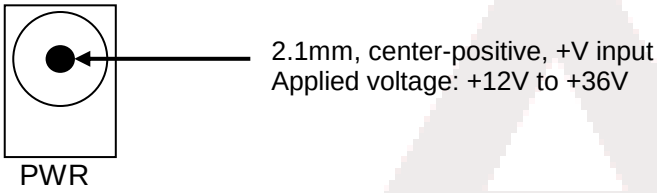
ON_OFF Switch

The ON_OFF toggle switch provides ignition on and off control to the MC33730 supply. The MC33730 device enables and disables the main power supplies. With the switch in the ON position, all power indicators should light. Inspect input power connection and source, and fuse F1 if power indication does not occur.

PWR - Power Jack

The Power Jack provides the default power input to the board. The jack accepts a standard 2.1mm barrel plug connector, center-positive, to provide the +VIN supply of +12 to +36 volts DC.

Figure 2: PWR Jack – J9



Input Protection

Input current is limited by fuse F1. A 5x20mm, 1A slow-blow type fuse, protects the EVBMB for over current input conditions. An avalanche diode at D2 limits input voltage to 40V to protect the APSIC from damage.

VSTBY Switch

The VSTBY switch provides the voltage necessary to support the target MPU internal memory in stand-by mode. In the OFF position, the VSTBY input is connected to GND. In the ON position, VSTBY connects to the VKAM standby voltage from the MC33730 supply.

Cut-away option CT1 allows the user to isolate VSTBY from the switch. With CT1 open, the user must apply external battery or ground to the VSTBY position on the Power Port connector or I/O header ring.

Power Port

Power Port provides access to the main power supplies and MC33730 optional supplies. Note that the +VIN connection provided at pin 1 is not switched by the ON-OFF switch or fused and is directly connected to the Power Jack.

Figure 3: POWER PORT – J10

PIN #		SIGNAL DESCRIPTION
1	2	+VIN – DC input voltage from PWR jack (NO fuse or polarity protection).
3	4	+5V = regulated +5V supply from MC33730
5	6	+3.3V = regulated +3.3V supply from MC33730
7	8	+1.2V = regulated +1.5V supply from MC33730
9	10	VDD = MPC567X VDD supply, 1.2V typically
11		VREF1 = MC33730 Optional 5V reference supply.
	12	+5VA = MC33730 VREF2 output dedicated to the MPC567X 5V analog supply.
13		RST3* = 3.3V power supply reset signal to the MC33730 supply.
	14	VSTBY = standby voltage applied to target MPC567X VSTBY input
15		RSTL* = 1.2V power supply reset signal from MC33730 supply.
	16	REGON = control signal to the M33730, see MC33730 user guide.
17		RSTH* = 5V power supply reset signal to the MC33730 supply.
	18	IGN_ON = control signal output from the MC33730, see MC33730 user guide.
19		RSTKAM* = Keep Alive / VSTBY / backup power supply reset signal to the MC33730.
	20	PFD = control signal output from the MC33730, see MC33730 user guide.
21	22	Ground / VSS

Analog Supplies

The VREF2 output from the MC33730 supplies the analog voltage (+5VA) to the target MCU. This voltage is available at the daughter card stack header.

USER COMPONENTS

The EVBMB provides 8 LED indicators, one 8-position DIP switch, 4 push switches, a loud-speaker with amplifier, and 2 user potentiometers. These devices are accessed via the USER LED, USER SWITCH, and USER DEV I/O headers. These user devices are useful to evaluate operation and assist in code development.

USER_LED

The USER_LED header provides control access to the user LED1 TO LED8. Connector pin-1 connects to LED1; connector pin-2 connects to LED2; etc… A buffer at each LED reduces the drive current requirement to approximately 300uA. Each LED turns ON when a high voltage level is applied to the respective USER_LED input pin. Figure 4 below shows the pin-out for the USER_LED option connector.

Figure 4: USER_LED – J5

PIN #	LED Connection
1	LED1
2	LED2
3	LED3
4	LED4
5	LED5
6	LED6
7	LED7
8	LED8

USER_SWITCH

The USER_SWITCH option header provides access to the 8-position DIP Switch. Connector pin-1 connects to switch position 1; connector pin-2 connects to switch position 2; etc… In the OFF position, a 10K ohm resistor pulls each switch position low. In the ON position, each switch position connects 3.3V to the connector pin. Figure 5 below shows the pin-out for the USER_SWITCH option connector.

Figure 5: USER_SWITCH – J8

PIN #	DIP SW Connection
1	SW5-1
2	SW5-2
3	SW5-3
4	SW5-4
5	SW5-5
6	SW5-6
7	SW5-7
8	SW5-8

USER_DEV

User DEV provides access to the 4 push switches (SW1 – SW4), loud-speaker, and 2 user potentiometers (RV1 and RV2). Figure 6 below shows the pin-out for the USER_DEV option connector.

Figure 6: USER_DEV – J4

PIN #	Label	USER COMPONENT CONNECTION
1	1	SW1 out, de-bounced CMOS, drive 0 or 3.3V, active low.
2	1D	SW1 out, de-bounced Open Drain output, active low, 10K ohm pull-up to 3.3V. Suitable for IRQ input signal drive.
3	2	SW2 out, active low, 10K ohm pull-up to 3.3V.
4	3	SW3 out, active low, 10K ohm pull-up to 3.3V.
5	4	SW4 out, active low, 10K ohm pull-up to 3.3V.
6	SP	SPEAKER amp input. 0 to 5Vpp, volume adjust with SPKR_VOL.
7	R1	RV1 center tap, 0 – 5V adjustment
8	R2	RV2 center tap, 0 – 5V adjustment

SW1 – SW4 Push Switches

The push-button switches provide momentary active low input for user applications. SW1 provides the additional feature of a de-bounced output providing glitch-free operation and push-pull output on pin 1 or open drain output on pin 2. Typical user application would be to provide program control or menu selection input.

SW2 – SW4 provide momentary, active low, input to the MCU. Each SW is pulled to 3.3V through a 10K ohm resistor. Refer to Figure 6 above.

Speaker

A speaker with amplifier allows user applications to generate sound effects from a target MCU output. The amplifier generated frequencies between 300Hz to 10 KHz. The SPKR_VOL potentiometer provides speaker volume adjustment. The amplifier may optionally be disabled by the target MCU using the SHDN input on the amplifier. A logic high input on SHDN disables the amplifier. Refer to Figure 6 above.

User Potentiometers

The user Potentiometers provide an adjustable linear voltage output from 0 to 5V. The voltage signal may be applied to the target MCU analog input port for user application development. Potentiometer output is filter to remove unwanted high-frequency behavior. Refer to Figure 6 above.

COMMUNICATIONS PORTS

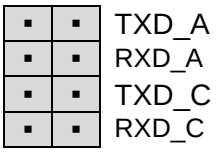
COM Ports

An RS-232 transceiver provides RS-232 to TTL/CMOS logic level translation between the COM1 and COM2 connectors and the MCU. A standard DB-9, right-angle connector is applied at COM1. A ferrite bead on shield ground provides conducted immunity protection. A 10-pin, 0.1” spacing, pin-header is applied at COM2 RTS and CTS are looped on both COM1 and COM2 connectors.

COM_EN

The COM_EN option header individually connects and disconnects TXD and RXD signals between the MCU and the transceiver. Removing a shunt disconnects the associated signal. Installing a shunt connects the associated signal. Figure 7 shows shunt setting for the COM_EN option header.

Figure 7: COM_EN Option Header – JP1

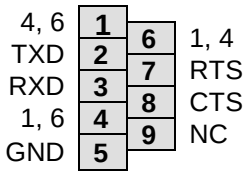


Shunt	
On	Off
Enabled	Disabled
Enabled	Disabled
Enabled	Disabled
Enabled	Disabled

COM Connectors

A standard 9-pin Dsub connector provides external connections for COM1. The Dsub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. Figure 8 below shows the DB9 connector pin-out.

Figure 8: COM1 Connector – J1

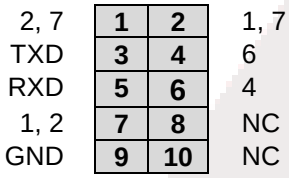


Female DB9 connector that interfaces to the target MCU via the RS232 transceiver.

Pins 1, 4, and 6 are connected together.

A standard “Berg” pin header on 0.1” centers provides external connections for COM2.

Figure 9: COM2 Connector – J2



CAN Port

A TJA1054T CAN physical transceiver (PHY) is applied to support CAN communications. Each of 3 CAN outputs from the target MCU are applied to the CAN PHY through the CAN_SEL option header. A 4-pin MOLEX connector interfaces to external CAN cabling. The user may apply multiple CAN channel to the transceiver if the open drain TX output type is applied on the associated CAN channel transmit pins.

The differential CAN signals are terminated by 120. This termination may be removed using the option jumpers at JP3. Avalanche diodes protect the CAN PHY from voltage surges on the input differential signal lines. Figure 10 below shows the CAN connector pin-out.

Figure 10: CAN_PORT – J3

Pin	TJA1040 CAN Transceiver Signal
1	CANL
2	CANH
3	NC
4	NC

NOTE: CAN Port Connector – Molex 39-30-3045

Mates with; Housing – Molex 39-01-4040, Pin – Molex 39-00-0036

CAN_SEL Option

The CAN_SEL option header allows selection of the MPC5554 CAN channels applied to the CAN transceiver and CAN Port. To use multiple input transmit channels, configure the channel for open-drain operation. Figure 11 below shows the CAN_SEL pin-out.

Figure 11: CAN_SEL – JP2

Position	Signal	Description
2	CNTX_A	CAN Channel A TX output (**DEFAULT**)
4	CNRX_A	CAN Channel A RX input (**DEFAULT**)
6	CNTX_B	CAN Channel B TX output
8	CNRX_B	CAN Channel B RX input
10	CNTX_C	CAN Channel C TX output
12	CNRX_C	CAN Channel C RX input
14	CNRX_D	CAN Channel D TX output
16	CNRX_D	CAN Channel D RX input

FlexRay Ports

The MPC567XEVBMB supports 2 FlexRay communication channels at the FlexRay_A and FlexRay_B connectors. The FLEXRAY option header connects the target MCU to the FlexRay transceivers. Cut-traces at the FLEXRAY option header provide default connection but allow optional configurations. Access to FlexRay transceiver status and control signals are available at though-hole vias located adjacent to the transceiver. Refer to the target MCU and TJA1080 device reference manuals for details of FlexRay operation.

FR_SEL Option

Target MCU FlexRay I/O signals are provided to TJA1080 transceiver devices by the FLEXR_SEL option. This option is hardwired to enable the signal connections. To isolate the signals, the FLEXR_SEL options maybe cut and a .1 grid 2 x 6 header pin option block installed to apply option jumpers.

Figure 12: FR_SEL – J15

Position	Signal	Description
1	FR_A_TX	FlexRay Channel A transmit
2	FR_A_RX	FlexRay Channel A receive
3	FR_A_TXEN	FlexRay Channel A transmit enable
4	FR_B_TX	FlexRay Channel B transmit
5	FR_B_RX	FlexRay Channel B receive
6	FR_B_TXEN	FlexRay Channel B transmit enable

Transceiver Test Pads

Test pads provide access to the FlexRay transceiver status and control pins. User may connect the target MCU I/O signals to the test pads to enhance FlexRay operation. Test Pads surround the devices on the EVB board and are indicated by FR21 or FR22 on the EVB board schematic.

Figure 13: FlexRay Transceiver Test Pads

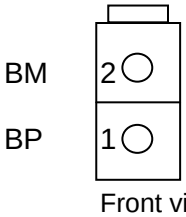
Rev A Label	Pin	TJA1080 FlexRay Transceiver Signal
1	1	Inhibit 2 output
2	2	Inhibit 1 output
3	3	Enable, pulled high – active
4	5	TX Data input, also FLEXR option 1 or 4
5	6	TX Enable Input, also FLEXR option 3 or 6
6	7	RX Data output, also FLEXR option 2 or 5
7	8	Bus Guardian Enable Input, pulled high
8	9	Standby Input, pulled high
9	10	TXD1, star connection I/O, pulled low.
13	11	TXD0, star connection I/O, pulled low.
12	12	RX Active Output
11	13	Error Output
10	15	Wake Input

NOTE: Test Pad silkscreen labels are incorrect. The table above shows the correct connection between the Revision A silkscreen and the associated FlexRay transceiver pin.

FlexRay Connectors

Input FlexRay signals are terminated by 94 ohm. This termination may be removed using option jumper JP5. Vertical, 2-position Molex connectors attach to external FlexRay cabling.

Figure 14: LIN Connector – J11



Front view (looking into connector)

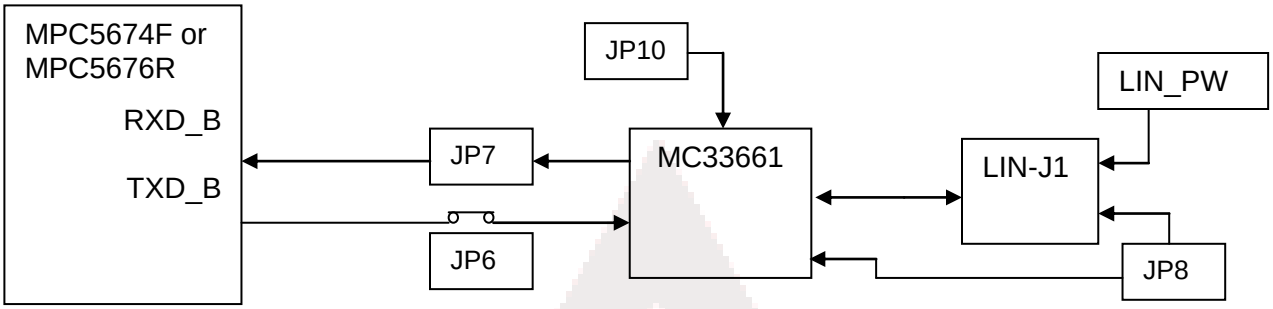
NOTE: FlexRay Port Connector – Molex 39-29-1028

Mates with; Housing – Molex 39-01-2020, Pin – Molex 39-00-0036

LIN Port

The LIN_J1 port provides a Master Mode LIN network connection. The target MCU acts as a LIN Master node on the LIN Network. A LIN physical layer transceiver U7 (MC33661, or equivalent) is provided between the target MCU and the LIN network connector. Refer to the LIN PHY data sheet for complete details of transceiver operation. The following diagram shows the LIN connection:

Figure 15: LIN Block Diagram



The LIN interface provides optional features of slew rate control, network supply, and wake up option. Refer to the MC33661 Reference Manual for detail on PHY functionality. The following sections detail functionality for LIN option jumpers.

LIN Enable Option

LIN_EN is routed to a test-point via located adjacent to the device. This input signal is pulled up by default to enable transceiver operation. Connect a target MCU GPIO signal to this via to provide MCU control of transceiver functionality.

JP6 Option

JP5 connects the target MCU signal, RXD_B, input to the LIN transceiver. A cut-trace at this location provides default connection. A header pin is not installed at this location in default configurations.

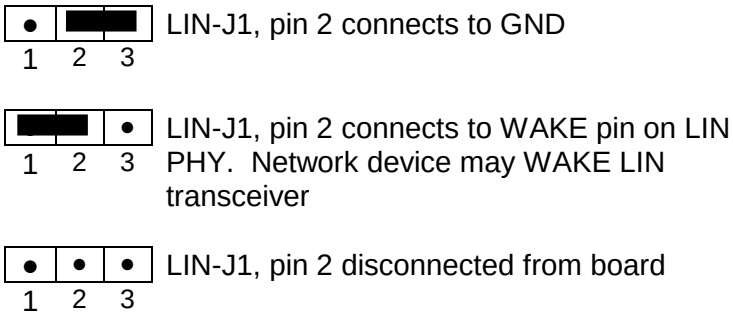
JP7 Option

JP7 connects the target MCU signal, TXD_B to the LIN transceiver. An option jumper at this location allows the user to isolate the target MCU pin from the LIN transceiver.

JP9 Option

LIN-J1 connector pin 2 may be configured for different network requirements by use of option header JP4. Removing the JP4 shunt disconnects LIN-J1 pin 2 from the EVB board.

Figure 16: Option Header – JP4



LIN_PWR Option – JP8

The LIN_PWR option jumper connects J11-1 to the unfused, +V input on the EVBMB. This allows the EVBMB to function as a LIN slave device and draw power from the LIN network. In this configuration, external power should not be applied at the PWR jack.

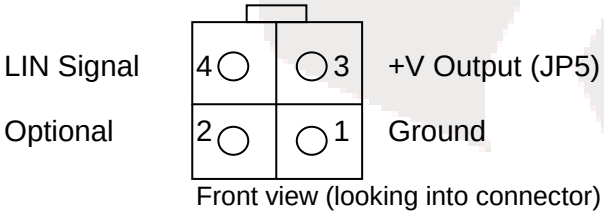
MSTR Option – JP10

The MSTR option jumper at JP10 allows the LIN transceiver to be configured for master mode functionality. The MC33661 also support Master-Mode functionality using the INH pin. Refer to the MC33661 device datasheet for details on use and configuration.

LIN-J1 Connector

The LIN-J1 network connector provides a standard pin configuration with a network option position on pin 2.

Figure 17: LIN Connector – J11



NOTE: LIN Port Connector – Molex 39-29-1048

Mates with; Housing – Molex 39-01-2040, Pin – Molex 39-00-0036

PROTOTYPE AREA

An area of thru-holes measuring 26x24 holes, spaced on 0.1” centers, is provided to support circuit prototyping and debug. GND is applied on 3 sides of the prototyping area. A row of +5V and +3.3V is also available along 1 edge.

EVBMB I/O PORT ACCESS HEADERS

The standard IO Header Ring is modified for EVBMB. IO signals from the target MCU are grouped by functionality. Access pin headers consist of dual-row, 0.1" pin headers of varying pin count. The following figures detail the pin-out for each IO Port Access Header. Only the primary signal name is included in the figures below.

Figure 18: Analog Access Port Headers

J18

+5VA	1	2	VSSA
ANA_0	3	4	ANA_1
ANA_2	5	6	ANA_3
ANA_4	7	8	ANA_5
ANA_6	9	10	ANA_7
ANA_8	11	12	ANA_9
ANA_10	13	14	ANA_11
ANA_12	15	16	ANA_13
ANA_14	17	18	ANA_15
ANA_16	19	20	ANA_17
ANA_18	21	22	ANA_19
ANA_20	23	24	ANA_21
ANA_22	25	26	ANA_23
VRH	27	28	VRL
+5VA	29	30	VSSA

AN_A

J19

+5VA	1	2	VSSA
ANB_0	3	4	ANB_1
ANB_2	5	6	ANB_3
ANB_4	7	8	ANB_5
ANB_6	9	10	ANB_7
ANB_8	11	12	ANB_9
ANB_10	13	14	ANB_11
ANB_12	15	16	ANB_13
ANB_14	17	18	ANB_15
ANB_16	19	20	ANB_17
ANB_18	21	22	ANB_19
ANB_20	23	24	ANB_21
ANB_22	25	26	ANB_23
VRH	27	28	VRL
+5VA	29	30	VSSA

AN_B

J20

+5VA	1	2	VSSA
AN_24	3	4	AN_25
AN_26	5	6	AN_27
AN_28	7	8	AN_29
AN_30	9	10	AN_31
AN_32	11	12	AN_33
AN_34	13	14	AN_35
AN_36	15	16	AN_37
AN_38	17	18	AN_39

AN

Figure 19: TPU Access Port Headers

J22

TPU_A0	1	2	TPU_A1
TPU_A2	3	4	TPU_A3
TPU_A4	5	6	TPU_A5
TPU_A6	7	8	TPU_A7
TPU_A8	9	10	TPU_A9
TPU_A10	11	12	TPU_A11
TPU_A12	13	14	TPU_A13
TPU_A14	15	16	TPU_A15
TPU_A16	17	18	TPU_A17
TPU_A18	19	20	TPU_A19
TPU_A20	21	22	TPU_A21
TPU_A22	23	24	TPU_A23
TPU_A24	25	26	TPU_A25
TPU_A26	27	28	TPU_A27
TPU_A28	29	30	TPU_A29
TPU_A30	31	32	TPU_A31
TCRCLK_A	33	34	NC
+3.3V	35	36	GND

AN_B

J23

TPU_B0	1	2	TPU_B1
TPU_B2	3	4	TPU_B3
TPU_B4	5	6	TPU_B5
TPU_B6	7	8	TPU_B7
TPU_B8	9	10	TPU_B9
TPU_B10	11	12	TPU_B11
TPU_B12	13	14	TPU_B13
TPU_B14	15	16	TPU_B15
TPU_B16	17	18	TPU_B17
TPU_B18	19	20	TPU_B19
TPU_B20	21	22	TPU_B21
TPU_B22	23	24	TPU_B23
TPU_B24	25	26	TPU_B25
TPU_B26	27	28	TPU_B27
TPU_B28	29	30	TPU_B29
TPU_B30	31	32	TPU_B31
TCRCLK_B	33	34	NC
+3.3V	35	36	GND

AN_A

J24

TPU_C0	1	2	TPU_C1
TPU_C2	3	4	TPU_C3
TPU_C4	5	6	TPU_C5
TPU_C6	7	8	TPU_C7
TPU_C8	9	10	TPU_C9
TPU_C10	11	12	TPU_C11
TPU_C12	13	14	TPU_C13
TPU_C14	15	16	TPU_C15
TPU_C16	17	18	TPU_C17
TPU_C18	19	20	TPU_C19
TPU_C20	21	22	TPU_C21
TPU_C22	23	24	TPU_C23
TPU_C24	25	26	TPU_C25
TPU_C26	27	28	TPU_C27
TPU_C28	29	30	TPU_C29
TPU_C30	31	32	TPU_C31
TCRCLK_C	33	34	NC
+3.3V	35	36	GND

AN_A

Figure 20: EMIOS, COM, & CONFIG Access Port Headers

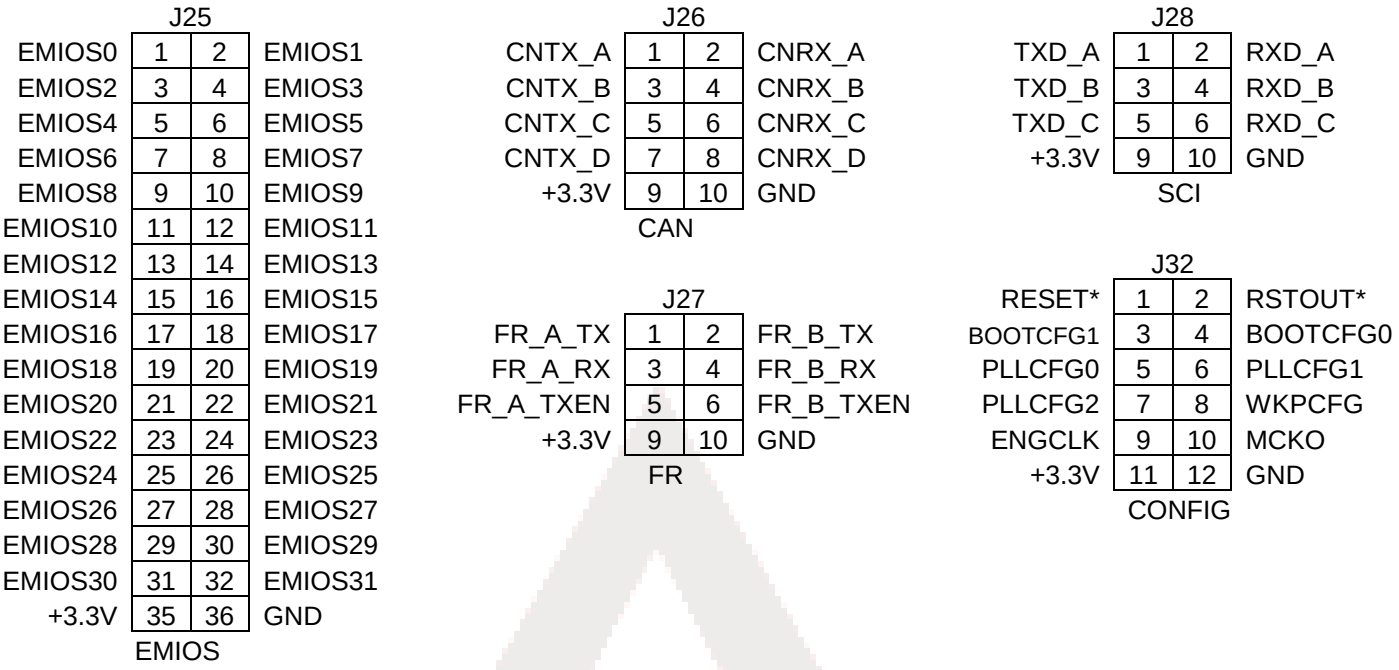


Figure 21: DSPI Access Ports