# MPC5674ADAT324

Demonstration Module for Freescale MPC5674 Microcontroller

# Hardware User Guide

**Web Site:** www.axman.com

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# REVISION

| Date | Rev | Comments |
|---|---|---|
| August 3, 2010 | A | Initial Release |

# CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be applied whenever handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing reserves the right to make changes without further notice to any products to improve reliability, function or design. Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the MPC5561EVB board:

   a) This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

# TERMINOLOGY

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

Jumper on, in, or installed – jumper or shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle – jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Signal names followed by an asterisk (*) denote active-low signals.

# OVERVIEW

The MPC5674ADAT324 (ADAT324) supports the MPC5674 microcontroller in the 324BGA package. The ADAT324 is a daughter-card type module which is designed to mount directly to the MPC5674FXMB (FXMB) via 4, low-profile stack headers. This document details the hardware configuration for the ADAT324.

# POWER SUPPLY

Primary power to the ADAT324 is provided through the stack headers. Alternate power input may be applied through the power input at location J5. Location J5 is designed to accept 3.5mm terminal block. However, this terminal block is not installed in the default configuration.

Alternate power input allows the ADAT324 to be used as a stand-alone development module.

The MPC5674 VDD input is generated on-board using either a linear pass transistor at Q1 or a switch-mode power supply regulator at Q2. Option header at JP9, REGCTL selects either the linear regulator or the switch-mode regulator.

**CAUTION**
Disconnect power to the FXMB before installing the ADAT324; otherwise, damage to the ADAT324 and FXMB may otherwise occur.

## ANALOG Supplies

Analog voltage (+5VA) to the ADAT324 is provided from the FXMB via the 4 board stack headers. This voltage is not generated on the ADAT324 module. The VRH_EN option header selects +5VA by default. A cut-trace enables this option by default and the jumper is not installed in default configurations.

Analog voltage, +5VA, is not available with the module powered as a stand-alone module.

# OPTION JUMPERS

The following sections describe the functionality of each option jumper from a hardware standpoint only. Refer to the MPC5674 Reference Manual for further details on use and configuration of each option below.

## VDDEH_SEL – JP1

The VDDEH_SEL option jumper selects the high-voltage input applied to the target MCU. All target MCU VDDEH inputs are supplied by this option jumper. This option jumper is configured for +5V operation by default.

## EXTAL_SEL– JP2

The EXTAL_SEL option jumper selects between the on-board, 40 MHz crystal oscillator and the clock oscillator socket at X1 as timing input to the target MCU. This option jumper is configured for on-board crystal input by default.

## JP3

The JP3 option jumper applies +3.3V power to the OSC socket at X1. This option is enabled by default.

## VRH_EN– JP4

The VRH_EN option jumper applies +5VA to the VRH input on the target MCU. This option jumper is enabled by default.

## VDDSYN_EN– JP5

The VDDSYN_EN option jumper allows the end-user to configure VDD33 and VDDSYN to the target MCU. By default, this option jumper is configured to connect the VDDSYN output to the VDD33 input on the target MCU. This option jumper is not installed in default configurations.

## VDDREG_SEL– JP6

The VDDREG_SEL option jumper connects either +5V or +3.3V to the VDDREG input on the target MCU. By default, the option jumper is configured to connect +5V to the VDDREG input.

## VSTBY_SEL– JP7

The VSTBY_SEL option jumper enables or disables internal memory stand-by voltage to the target MCU. By default, the option jumper is configured to disable the VSTBY input.

## REGCTL– JP9

The REGCTL option jumper selects between the on-board linear regulator and the on-board switch-mode power supply. This option jumper is configured to select the linear regulator by default.

## MDOx Option Jumpers – JP12 thru JP27

The MDOx option jumpers, JP12 through JP27 connect the MDO[15:0] signals from the target MCU to the board stack header at P1. These option jumpers are enabled by default.

# DEVELOPMENT PORTS

The ADAT324 applies 1 JTAG and 1 Mictor NEXUS type development ports. Only one type of development cable should be used during any given development. Both development ports share several signals. A CBTLV3861 device buffers development port input and power signals protecting the target MCU from damage by transient input. This buffer provides a bi-directional 5 ohms series resistance on the input signals when powered on. The buffer also provides signal isolation when powered off.

To ensure proper communications, the ADAT324 and development cable must be powered in the proper sequence. Use the following power sequence to connect a development cable.

The power sequence shown below should be used when connecting a development cable to the ADAT324. This sequence should be used if the ADAT324 is mated to the FXMB or used in a stand-alone configuration.

## ADAT324 Power Sequence

1) Ensure power is switched OFF
2) Connect development port cable to the desired development port
3) Apply power to the target board.
4) If power is removed or the ON-OFF switch is turned off, remove development cable from board connector and re-apply from step 1 of this procedure.

# JTAG Port

The JTAG port provides a Freescale standard JTAG connection to the target MCU. The connector is a standard 2x7, 0.1" space, keyed box header. Example compatible cables include the OCDEMON™ NP-JTAG OnCE "Wiggler" and the P&E Microcomputer Systems CABPPCNEXUS. Host software supporting each cable must be used.

**Figure 1: JTAG Port Connector**

| Signal | | | Signal |
|---|---|---|---|
| B_TDI | 1 | 2 | GND |
| TDO | 3 | 4 | GND |
| B-TCK | 5 | 6 | GND |
| B_EVTI* | 7 | 8 | JTG8 TP |
| B-RESET* | 9 | 10 | B_TMS |
| B_+3.3V | 11 | 12 | GND |
| B_RDY* | 13 | 14 | B_JCOMP |

Notes:
1. B_… signals are buffered.
2. JTG8 TP signal is not connected to the target MCU. This pin connects to a test pad on the board.
3. All development cables may not support the B_EVTI* signal. Option CT5 cut will isolate this signal if not supported by the development cable.
4. Signals followed by a "*" symbol are active-low logic.

# NEXUS Port

The NEXUS port provides a more powerful, faster development port for use with high-end tools. The port connector is an AMP 38-pin Mictor style, part number 767053-1.

**Figure 2: NEXUS PORT**

| Signal | | | Signal |
|---|---|---|---|
| NXS1 TP | 1 | 2 | NXS2 TP |
| NXS3 TP | 3 | 4 | NXS4 TP |
| MDO9 | 5 | 6 | CLKOUT |
| BOOTCFG1 | 7 | 8 | MDO8 |
| B_RESET* | 9 | 10 | B_EVTI* |
| TDO | 11 | 12 | B_+3.3V |
| MDO10 | 13 | 14 | B_RDY* |
| B_TCK | 15 | 16 | MDO7 |
| B_TMS | 17 | 18 | MDO6 |
| B_TDI | 19 | 20 | MDO5 |
| B_JCOMP | 21 | 22 | MDO4 |
| MDO11 | 23 | 24 | MDO3 |
| ERSTOUT* | 25 | 26 | MDO2 |
| NXS27 TP | 27 | 28 | MDO1 |
| NXS29 TP(3) | 29 | 30 | MDO0 |
| +V | 31 | 32 | EVTO* |
| +V | 33 | 34 | MCKO |
| NXS35 TP(3) | 35 | 36 | MSEO1* |
| B_VSTBY | 37 | 38 | MSEO0* |

Notes:
1) B_… signals are buffered.
2) NXSxx TP signals are not connected to the target MCU. The pin connects to a test pad on the board.
3) Signals followed by a “*” symbol are active logic low.