MPC5561EVB

Demonstration Board for Freescale MPC5561

Hardware User Guide

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REVISION

Date	Rev	Comments
April 13, 2007	A	Initial Release.
July 23, 2008	B	Updated title page and address

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be applied whenever handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing reserves the right to make changes without further notice to any products to improve reliability, function or design. Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the MPC5561EVB board:

   a) This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Signal names followed by an asterisk (*) denote active-low signals.

MPC5561EVB CONFIGURATION

CONFIG Switch

The CONFIG switch sets reset configuration options for the MPC5561 device. Switch position 1 enables configuration options. The OFF position applies a low input signal to the MCU. Th ON position applies a high signal to the MCU.

Table 1: Configuration Switch

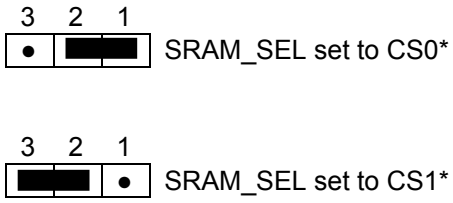
POS	SIGNAL	DEFAULT
8	Not connected	NA
7	WKPCFG	ON
6	PLLCFG2	ON
5	PLLCFG1	OFF
4	PLLCFG0	ON
3	BOOTCFG1	OFF
2	BOOTCFG0	ON
1	CONFIG enable	ON

NOTE: Refer to Freescale MPC5561 Documentation for detail on setting configuration options.

SRAM_SEL Option

The MPC5561EVB board provides a 1024K x 18 synchronous SRAM (U2) on the 15-bit data bus D[15:0]. SRAM_SEL provides selection of the CS0* or CS1* chip selects to access the external SRAM on the EVB board. Chip select configuration should be set for 0 wait states, 512K byte memory range, WE signals = Write Enable. The SRAM supports 4-word BURST mode access also.

Figure 1: SRAM_SEL



POWER SUPPLY

The primary power supply is the MC33730 APSIC configured to support the MPC5561 device. The MPC5561 VRC regulator provides the VDD (1.5V) supply in the default configuration. The MC33730 1.5V supply may be applied by optional configuration to provide the VDD 1.5V supply (CT1 short and CT2 open).

Power supply Reset signals for the 5V, 1.5V and 3.3V supplies are applied to the MPC5561 RESET* input by the closed S1 – S3 option pads respectfully. The open S0 option pad may apply the RSTKAM* back-up supply reset signal if closed by the user. Also see the POWER_PORT connection and MC33730 data sheet for power supply access details.

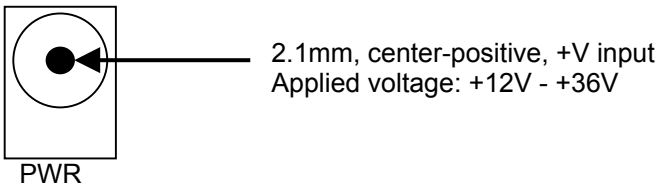
ON_OFF Switch

The ON_OFF toggle switch provides ignition on and off control to the MC33730 supply. The MC33730 device will enable and disable the main power supplies. With the switch in the ON position, all power indicators should light. Inspect input power connection and source, and fuse F1 if power indication does not occur.

PWR - Power Jack

The Power Jack provides the default power input to the board. The jack accepts a standard 2.0 ~ 2.1mm center barrel plug connector (positive voltage center) to provide the +VIN supply of +12 to +36 volts DC.

Figure 2: PWR Jack



FUSE – F1

Input power is limited by fuse F1. A 5x20mm, 1A slow-blow type fuse, protects the EVB board for over voltage input conditions.

VSTBY SWITCH

The VSTBY switch provides the voltage necessary to support the MPC6651 internal memory in stand-by mode. In the OFF position, the VSTBY input is connected to GND. In the ON position, the VSTBY input is connected to the 1V VKAM standby voltage from the MC33730 supply.

Cut-away option CT9 allows the user to isolate the VSTBY pin of the MPC5561 from the switch. With CT9 open, the user must apply external battery or ground to the VSTBY position on the Power Port connector or I/O header ring.

POWER PORT

Power Port provides access to the main power supplies and MC33730 optional supplies. Note that the +VIN connection provided at pin 1 is not switched by the ON-OFF switch or fused and is directly connected to the Power Jack.

Table 2:POWER PORT

PIN #		SIGNAL DESCRIPTION
1	2	+V IN= DC input voltage from PWR jack (NO fuse or polarity protection).
3	4	+5V = regulated +5V supply from MC33730
5	6	+3.3V = regulated +3.3V supply from MC33730
7	8	+1.5V = regulated +1.5V supply from MC33730
9	10	VDD = MPC5561 VDD supply, 1.5V typically
11		VREF1 = MC33730 Optional 5V reference supply.
	12	+5VA = MC33730 VREF2 output dedicated to the MPC5561 5V analog supply.
13		RST3* = 3.3V power supply reset signal from MC33730 supply.
	14	VSTBY = 1V backup / standby voltage applied to MPC5561 VSTBY input. See VSTBY_SW and CT15 option also.
15		RSTL* = 1.5V power supply reset signal from MC33730 supply.
	16	REGON = control signal to the M33730, see MC33730 user guide.
17		RSTH* = 5V power supply reset signal from MC33730 supply.
	18	IGN_ON = control signal output from the MC33730, see MC33730 user guide.
19		RSTKAM* = Keep Alive / VSTBY / backup power supply reset signal from the MC33730.
	20	PFD = control signal output from the MC33730, see MC33730 user guide.
21	22	Ground / VSS

ANALOG Supplies

The MC33730 VREF2 regulator output provides the MCU VDDA input supply (+5V) by default. Installing the VRH_EN option header also connects this source to the MPC5561 VRH input in default configuration. The MCU VRL input connects to GND by default through cut-trace VRL_EN. To apply external VRH, simply remove the VRH_EN shunt and connect an external voltage to the appropriate IO header ring pin. To apply external VRL or precision GND, simply open the VRL_EN cut-trace and connect an external voltage to the appropriate IO header ring pin.

The eQADC digital supply connects to +5V by default through cut-trace CT8. An optional connection to +3.3V for the eQADC is provided by CT7. Open CT8 prior to connecting CT7 for +3.3V operation. Consult the MPC5561 user manual for details on operating the eQADC at +3.3V and for limitations of the VDDA and VRH supplies.

PDI PORT

A VME connector at PDI PORT is included on the MPC5561EVB to allow PDI camera board access. The PDI connector is routed to the MPC5561 and a Xilinx FPGA through bus FET switches at U17, U19, and U25. Interface to the PDI connector is mutually exclusive with either the MCU controlling the port or the FPGA controlling the port. The PDI_EN option header allows either the MCU or the FPGA to control the interface. Control of the PDI connector is mutually exclusive., a shunt should always be installed at PDI_EN to ensure proper access to the PDI connector.

Table 3: PDI Connector

	C	B	A
1	GND	GND	GND
2	P_DATA1	GND	P_DATA0
3	P_DATA3	GND	P_DATA2
4	P_DATA5	GND	P_DATA4
5	P_DATA7	PDI_CHSEL0	P_DATA6
6	PDI_LINE_VALID	PDI_CHSEL1	PDI_SENSOR_CLK
7	ENGCLK	PDI_CHSEL2	PDI_FRAME_VALID
8	TPU_A7	GND	TPU_A0
9	P_DATA9	GND	GPIO206
10	TPU_A22	GND	GPIO207
11	TPU_A31	+1.5V	P_DATA8
12	TRCLK_A	GND	P_DATA10
13	P_DATA11	+5V	P_DATA12
14	P_DATA13	GND	P_DATA14
15	P_DATA15	GND	GND
16	+3.3V	+3.3V	+3.3V

A Xilinx Spartan 2 FPGA is included to interface to support alternate development access to the PDI port. A configuration EEPROM is provided to allow FPGA startup from RESET or POR. Default configurations do not include either the FPGA or EEPROM devices. Unused FPGA IO pins are routed to an I_O header providing additional development access if necessary.

Table 4: I_O Connector

	I_O		
I/O3	1	2	I/O4
I/O6	3	4	I/O7
I/O8	5	6	I/O10
I/O27	7	8	I/O29
I/O30	9	10	I/O31
I/O33	11	12	I/O34
I/O35	13	14	I/O36
I/O40	15	16	I/O41
I/O42	17	18	I/O43
I/O44	19	20	I/O45
I/O46	21	22	I/O47
I/O48	23	24	I/O49
I/O55	25	26	I/O56
I/O57	27	28	I/O58
I/O59	29	30	I/O60
I/O63	31	32	I/O73
I/O75	33	34	I/O81
I/O84	35	36	I/O94
I/O97	37	38	I/O98
I/O99	39	40	I/O100
I/O101	41	42	I/O109
I/O111	43	44	I/O115
I/O125	45	46	I/O181
I/O187	47	48	NC

USER COMPONENTS

The EVB board provides 8 LED indicators, one 8-position DIP switch, 4 push switches, a speaker with amplifier, and 2 user potentiometers. These devices are accessed via the USER LED, USER SWITCH, and USER DEV I/O headers. EVB board user may connect these user devices to the MPC5561 I/O header signals to evaluate operation or assist in code development.

USER_LED

The USER_LED header provides control access to the user LED1 TO LED8. Connector pin-1 connects to LED1; connector pin-2 connects to LED2; etc … A buffer at each LED reduces the drive current requirement to approximately 300uA. Each LED turns ON for voltages between 2.5V and 5V at the respective input pin.

USER_SWITCH

The USER_SWITCH option header provides access to the 8-position DIP Switch. Connector pin-1 connects to switch position 1; connector pin-2 connects to switch position 2; etc … In the OFF position, a 10K ohm resistor pulls each switch position low. In the ON position, each switch position connects 3.3V to the connector pin.

USER_DEV

User DEV provides access to the 4 push switches (SW1 – SW4), speaker, and 2 user potentiometers (RV1 and RV2).

Table 5: USER_DEV

PIN #	USER COMPONENT CONNECTION
1	SW1 out, de-bounced CMOS, drive 0 or 3.3V, active low.
2	SW1 out, de-bounced Open Drain output, active low, 10K ohm pull-up to 3.3V. Suitable for IRQ input signal drive.
3	SW2 out, active low, 10K ohm pull-up to 3.3V.
4	SW3 out, active low, 10K ohm pull-up to 3.3V.
5	SW4 out, active low, 10K ohm pull-up to 3.3V.
6	SPEAKER amp input. 0 to 5Vpp, volume adjust with SPKR_VOL.
7	RV1 center tap, 0 – 5V adjustment
8	RV2 center tap, 0 – 5V adjustment

SW1 – SW4 Push Switches

The push switches provide momentary active low input for user applications. SW1 has the additional feature of being de-bounced providing glitch-free operation and push-pull output on pin 1 or open drain output on pin 2. Typical user application would be to provide program control or menu selection input.

SW2 – SW4 provide momentary, active low, input to the MCU. Each SW is pulled to 3.3V through a 10K ohm resistor.

SPEAKER and SPKR_VOL

A speaker and amplifier allow user applications to generate sound effects from a MPC5561 output. The amplifier generated frequencies between 300Hz to 10Khz. The SPKR_VOL potentiometer provides speaker volume adjustment. The amplifier may optionally by disabled by the MPC5561 through the SHDN pad by applying a logic high input. The SHDN test pad must be connected to the appropriate MPC5561 IO signal.

USER POTENTIOMETERS

The user Potentiometers provide an adjustable linear voltage output from 0 to 5V. The voltage signal may be applied to an MPC5561 analog input port for user application development.

COMMUNICATION PORTS

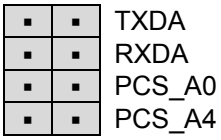
COM PORTS

An RS-232 transceiver provides RS-232 to TTL/CMOS logic level translation between the COM1 and COM2 connectors and the MCU. The COM1 connector is a 9-pin Dsub, right-angle connector. A ferrite bead on shield ground provides conducted immunity protection. The COM2 connector is a 10-pin header. RTS and CTS are looped on both COM1 and COM2 connectors.

COM_EN

The COM_EN option header individually connects and disconnects TXD and RXD signals between the MCU and the transceiver. Removing a shunt disconnects the associated signal. Installing a shunt connects the associated signal.

Figure 3: COM_EN Option Header

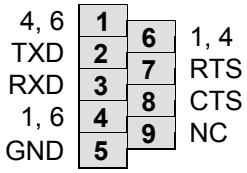


	Shunt	
	On	**Off**
TXDA	Enabled	Disabled
RXDA	Enabled	Disabled
PCS_A0	Enabled	Disabled
PCS_A4	Enabled	Disabled

COM Connectors

A standard 9-pin Dsub connector provides external connections for COM1. The Dsub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. The DB9 connector pin-out is shown below.

Figure 4: COM1 Connector

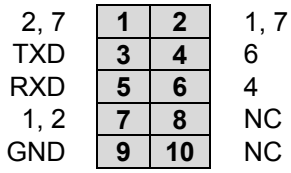


Female DB9 connector that interfaces to the MPC5561 via the RS232 transceiver.

Pins 1, 4, and 6 are connected together.

A standard “Berg” pin header on 0.1” centers provides external connections for COM2.

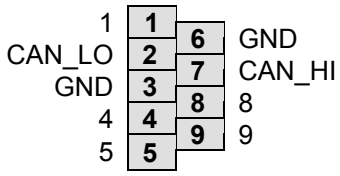
Figure 5: COM2 Connector



CAN Port

The CAN Port provides 9 pin connector with a TJA1050 CAN transceiver interface to the MPC5561 CAN channels. The CAN_SEL option locations select the CAN channel applied to the transceiver and CAN Port. User may apply more than one MPC5561 CAN channel to the port if the open drain TX output type is applied on the associated CAN channel transmit pins.

Figure 6: CAN_PORT



Female DB9 connector that interfaces to the MPC5561 via the CAN PHY

CAN_HI and CAN_LO signals are terminated differentially by 120 ohms. Test pads for all pin locations are located directly behind the CAN_PORT connector.

CAN_SEL Option

The CAN_SEL option header allows selection of the MPC5554 CAN channels applied to the CAN transceiver and CAN Port. To use multiple input transmit channels, configure the channel for open-drain operation.

Table 6: CAN_SEL

POSITION #	MPC5561 CAN SIGNAL
1	CNTX_A, channel A TX out (**DEFAULT**)
2	CNRX_A, channel A RX in (**DEFAULT**)
3	CNTX_B, channel B TX out
4	CNRX_B, channel B RX in
5	CNTX_C, channel C TX out
6	CNRX_C, channel C RX in

JP7 OPTION

JP7 provides user option access to the CAN transceiver control input. Default option position of 1-2 selected provides normal CAN transceiver operation. User may option CAN transceiver for Transmit control by moving JP7 option jumper to positions 2-3 and applying a MPC5561 output pin to JP7 pin 1. Transmit disable operation is active high.

FlexRay PORTS

The MPC5561EVB provides 2 FlexRay communication channels at the FlexRay_A and FlexRay_B connectors. Options are provided to isolate MPC5561 signals from the FlexRay ports and provide access to the transceiver status and control signals. Refer to the MPC5561 and TJA1080 device reference manuals for details of FlexRay operation.

FR_SEL Option

MPC5561 FlexRay I/O signals are provided to TJA1080 transceiver devices by the FLEXR_SEL option. This option is hardwired to enable the signal connections. To isolate the signals, the FLEXR_SEL options maybe cut and a .1 grid 2 x 6 header pin option block installed to apply option jumpers.

Table 7: FR_SEL

POSITION	MPC5561 SIGNAL
1	CNTX_B, FlexRay channel A Transmit Data Out
2	CNRX_B, FlexRay channel A Receive Data In
3	PCS_B2, FlexRay channel A Transmit Enable Out
4	eTPU_A4, FlexRay channel B Transmit Data Out
5	eTPU_A6, FlexRay channel B Receive Data In
6	eTPU_A5, FlexRay channel B Transmit Enable Out

Transceiver Test Pads

Test pads provide access to the FlexRay transceiver status and control pins. User may connect MPC5561 I/O signals to the test pads to enhance FlexRay operation. Test Pads surround the devices on the EVB board and are indicated by FR21 or FR22 on the EVB board schematic. The pads have a 2mm spacing so that header pins maybe installed.

Table 8: FlexRay TRANSCEIVER TEST PADS

Pin	TJA1080 FlexRay Transceiver Signal
1	Inhibit 2 output
2	Inhibit 1 output
3	Enable, pulled high – active
5	TX Data input, also FLEXR option 1 or 4
6	TX Enable Input, also FLEXR option 3 or 6
7	RX Data output, also FLEXR option 2 or 5
8	Bus Guardian Enable Input, pulled high
9	Standby Input, pulled high
10	TXD1, star connection I/O, pulled low.
11	TXD0, star connection I/O, pulled low.
12	RX Active Output
13	Error Output
15	Wake Input

FlexRay_A and FlexRay_B Connectors

FlexRay signals at the connectors are common mode noise filtered and terminated per Freescale specifications. The connectors are 1.27mm on-center, Molex 53048-0210 or equivalent . Use Molex 51021 series to mate to on-board connectors.

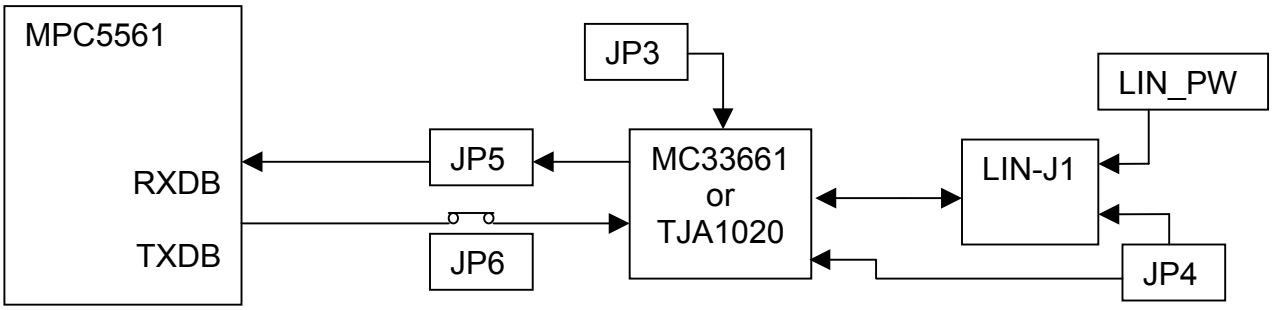
Table 9: FLEXRAY CONNECTORS

FLEXRAY Connector	FlexRay Signal
1	Bus Plus (+)
2	Bus Minus (-)

LIN_J1

The LIN_J1 port provides a Master Mode LIN network connection. The MPC5561 device acts as a LIN Master node on the LIN Network. A LIN physical layer transceiver U7 (MC33661, or equivalent) is provided between the MPC5561 device and the LIN network connector. Refer to the LIN PHY data sheet for complete details of transceiver operation. The following diagram shows the LIN connection:

Figure 7: LIN BLOCK DIAGRAM



The LIN interface provides optional features of slew rate control, network supply, and wake up option. See the JP4, JP5, JP6, JP7 and CT8 options following.

LIN ENABLE OPTION

MPC5561 I/O signal GPIO203 provides LIN transceiver U7 enable control (EN pin). Software control of the EN pin allows the user to set the slew rate control of the transceiver. User applications should configure the GPIO203 pin for output to operate the LIN transceiver. If GPIO203 is needed for other purposes, the CT10 cut-trace may be cut to isolate the signal from the LIN transceiver. JP3 option shunt may then be installed to enable the transceiver. Refer to the MC33361 data sheet for further details of operation.

JP3 Option

Installation of JP3 applies a pull-up resistor on the LIN transceiver enable pin. The MPC5561 GPIO205 may still control the transceiver enable operation when JP3 is installed.

JP5 OPTION

JP5 connects the MPC5561 signal, RXDB, input to the LIN transceiver. For LIN operation JP4 must be installed.

JP6 OPTION

JP6 is wired closed by default and not populated. JP5 connects the MPC5561 signal, TXDB, to the LIN transceiver. User may cut the JP5 wire trace to isolate the TXDB signal.

JP4 OPTION

LIN-J1 connector pin 2 may be configured for different network requirements by use of option header JP4. Removing the JP4 shunt disconnects LIN-J1 pin 2 from the EVB board.

Table 10: JP4 OPTION HEADER

● ▬ 1 2 3	LIN-J1, pin 2 connects to GND
▬ ● 1 2 3	LIN-J1, pin 2 connects to WAKE pin on LIN PHY
▬ ● 1 2 3	LIN-J1, pin 2 disconnected from board

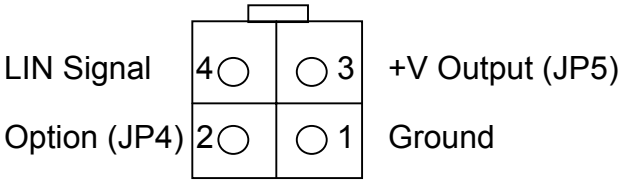
LIN_PWR Option

Installation of the LIN_PWR option applies MPC5561EVB +V input voltage for LIN network power to LIN-J1 pin 3. This connection allows the EVB board to operate as a LIN master node to power remote LIN slave nodes. User should use caution to not overload the F1 fuse and verify only one source is applied on the network.

LIN-J1 Connector

The LIN-J1 network connector provides a standard pin configuration with a network option position on pin 2.

Figure 8: LIN Connector



Front view (looking into connector from outside of board edge)

NOTE: Mating connector = Molex 39-01-2040 with 39-00-0039 pins.

DEVELOPMENT PORTS

The MPC5561EVB board provides 1 JTAG and 2 NEXUS type development ports. Only one of the development ports should be applied since common signals are used between the ports. The development port input and power signals are buffered by a CBTLV3861 device. This buffer provides a bi-directional 5 ohms series resistance on the input signals when powered on. The buffer also provides signal isolation when powered off.

To ensure proper communications, the MPC5561EVB and development cable must be powered in the proper sequence. Use the following power sequence to connect a development cable to the MCP5561EVB.

Figure 9: MPC5561EVB Power Sequence

1) MPC5561EVB board ON–OFF switch is OFF and no power is applied to the PWR connector.

2) Connect development port cable to the desired MPC5561EVB board development port.

3) Apply power to the MPC5561EVB board PWR connector and turn ON–OFF switch ON.

4) If power is removed or the ON-OFF switch is turned off, remove development cable from board connector and re-apply from step 1 of this procedure.

JTAG Port

The JTAG port provides a Freescale standard JTAG connection to the MPC5561. The connector is a standard 2x7, .1 inch pin space keyed pin header. Example compatible cables include the OCDEMON™ NP-JTAG OnCE “Wiggler” and the P&E Microcomputer Systems CABPPCNEXUS. Host software must be used to operate each cable.

Table 11: JTAG Port Connector

Signal			Signal
B_TDI	1	2	GND
TDO	3	4	GND
B-TCK	5	6	GND
B_EVTI*	7	8	JTG8 TP
B-RESET*	9	10	B_TMS
B_+3.3V	11	12	GND
B_RDY*	13	14	B_JCOMP

Notes:
1. B_… signals are buffered.
2. JTG8 TP signal is not connected to the MPC5554 and provides a Test Pad on the board.
3. All development cables may not support Pin 7 or the B_EVTI* signal. Option CT14 cut will isolate this signal if not supported by the development cable and issues are present.
4. Signals followed by a "*" symbol are active logic low.

NEXUS Port

The NEXUS port provides a more powerful and higher speed development port for high-end tools. The port connector is an AMP 38-pin Mictor style, part number 767053-1.

Table 12: NEXUS PORT

Signal			Signal
NXS1 TP	1	2	NXS2 TP
NXS3 TP	3	4	NXS4 TP
MDO9	5	6	CLKOUT
BOOTCFG1	7	8	MDO8
B_RESET*	9	10	B_EVTI*
TDO	11	12	B_+3.3V
MDO10	13	14	B_RDY*
B_TCK	15	16	MDO7
B_TMS	17	18	MDO6
B_TDI	19	20	MDO5
B_JCOMP	21	22	MDO4
MDO11	23	24	MDO3
ERSTOUT*	25	26	MDO2
NXS27 TP	27	28	MDO1
NXS29 TP(3)	29	30	MDO0
+V	31	32	EVTO*
+V	33	34	MCKO
NXS35 TP(3)	35	36	MSEO1*
B_VSTBY	37	38	MSEO0*

Notes:
1) B_… signals are buffered.
2) NXSxx TP signals are not connected to the MPC5561 and provide a Test Pad on the board.
3) NXSxx signal TP is also connected to the ROBUST Nexus connector.
4) Signals followed by a "*" symbol are active logic low.

ROBUST Port

The ROBUST port connector location is provided for user expansion. This port provides the ROBUST Nexus 51 pin location that applies the GLENAIR MR7580-51P2BNU connector. This connector is not installed in default configurations.

Table 13: ROBUST Port

Pin	Signal
1	+V
2	+V
3	B_VSTBY1
4	NXS35 TP
5	TDO
6	B_RDY*
7	B_RESET*
8	B_+3.3V
9	B_EVTI*
10	GND
11	B_JCOMP
12	GND
13	B_TMS
14	GND
15	B_TDI
16	GND
17	B_TCK
18	GND

Pin	Signal
19	MDO0
20	GND
21	MCKO
22	GND
23	EVTO*
24	GND
25	MSEO0*
26	MDO9
27	MDO1
28	GND
29	MDO2
30	GND
31	MDO3
32	GND
33	NXS29 TP
34	GND
35	MSEO1*

Pin	Signal
36	GND
37	MDO4
38	GND
39	MDO5
40	GND
41	MDO6
42	GND
43	MDO7
44	GND
45	MDO8
46	GND
47	MDO10
48	GND
49	MDO11
50	GND
51	JP1 pin 2

Notes:
1) NXS29 and NXS35 signals are also connected to the NEXUS connector.
2) Signals followed by a "*" symbol are active logic low.

JP1 Option

JP1 provides signal selection for the Robust Nexus connector pin 51. Position 1-2 provides the BOOTCFG1 signal and position 2-3 provides the ERSTOUT* signal.

Table 14: JP1 OPTION HEADER

●	▬		ERSTOUT* connected to ROBUST NEXUS, pin 51
1	2	3	
▬		●	BOOTCFG1 connected to ROBUST NEXUS, pin 51
1	2	3	

MPC5561 I/O HEADER RING

MPC5561 I/O signals are provided by the I/O header ring. The header ring consists of .1 inch grid pins organized in 4 rows for each side of the MPC5561 device. Each row reflects the corresponding location of the MPC5561 device BGA package ball ring. Signals indicated are the EVB board primary function.

Table 15: IO RING HEADER A1 - B4

	1	2	3	4
A	VSS	VDD	VSTBY	AN37
B	VDD33	VSS	VDD	AN36
C	ETPUA 30	ETPUA 31	VSS	VDD
D	ETPUA 28	ETPUA 29	ETPUA 26	VSS
E	ETPUA 24	ETPUA 27	ETPUA 25	ETPUA 21
F	ETPUA 23	ETPUA 22	ETPUA 17	ETPUA 18
G	ETPUA 20	ETPUA 19	ETPUA 14	ETPUA 13
H	ETPUA 16	ETPUA 15	ETPUA 10	VDDEH 1
J	ETPUA 12	ETPUA 11	ETPUA 6	ETPUA 9
K	ETPUA 8	ETPUA 7	ETPUA 2	ETPUA 5
L	ETPUA 4	ETPUA 3	ETPUA 0	ETPUA 1
M	BDIP	TCRCLKA	CS1	CS0
N	CS3	CS2	WE1	WE0
P	ADDR 16	ADDR 17	RD_WR	VDD33
R	ADDR 18	ADDR 19	VDDE2	TA
T	ADDR 20	ADDR 21	ADDR 12	TS
U	ADDR 22	ADDR 23	ADDR 13	ADDR 14
V	ADDR 24	ADDR 25	ADDR 15	ADDR 31
W	ADDR 26	VDDE2	ADDR 30	VSS
Y	ADDR 28	ADDR 27	VSS	VDD
AA	ADDR 29	VSS	VDD	VDDE2
AB	VSS	VDD	VDDE2	DATA0
	1	**2**	**3**	**4**

Table 16: IO RING HEADER A5 – D18

D	C	B	A	
VDD	AN8	AN39	AN11	**5**
AN38	AN17	AN19	VDDA1	**6**
AN9	AN20	AN16	VSSA1	**7**
AN10	AN21	AN0	AN1	**8**
AN18	AN3	AN4	AN5	**9**
AN2	AN7	REFBYPC	VRH	**10**
AN6	AN22	AN23	VRL	**11**
AN24	AN25	AN26	AN27	**12**
AN29	AN30	AN31	AN28	**13**
AN34	AN33	AN32	AN35	**14**
VDDEH 9	VDDA0	VSSA0	VSSA0	**15**
AN15	AN14	AN13	AN12	**16**
MDO6	MDO5	MDO9	MDO11	**17**
MDO3	MDO2	MDO7	MDO10	**18**
D	**C**	**B**	**A**	

Table 17: IO RING HEADER W5 – AB18

	AB	AA	Y	W
5	DATA2	DATA1	VDDE2	VDD
6	DATA3	VDDE2	DATA8	VDDE2
7	DATA4	GPIO 206	DATA9	VDD33
8	DATA6	DATA5	DATA10	VDDE2
9	OE	DATA7	GPIO 207	DATA11
10	EMIOS 0	VDDE2	DATA13	DATA12
11	EMIOS 1	EMIOS 3	DATA15	DATA14
12	EMIOS 4	EMIOS 5	EMIOS 6	EMIOS 2
13	EMIOS 7	EMIOS 9	EMIOS 10	EMIOS 8
14	EMIOS 11	EMIOS 13	EMIOS 15	VDDEH 4
15	EMIOS 14	EMIOS 16	EMIOS 17	EMIOS 12
16	EMIOS 18	EMIOS 19	EMIOS 22	EMIOS 21
17	EMIOS 20	EMIOS 23	CNTXA	VDDE5
18	CNTXB	CNRXA	VDDE5	NC
	AB	**AA**	**Y**	**W**

Table 18: IO RING HEADER A19 – AB22

19	20	21	22	
MDO8	VDD	VDD33	VSS	**A**
MDO4	MDO0	VSS	VDDE7	**B**
MDO1	VSS	VDDE7	VDD	**C**
VSS	VDDE7	TCK	TDI	**D**
VDDE7	TMS	TDO	TEST	**E**
VDDE7	JCOMP	EVTI	EVTO	**F**
RDY	MCKO	MSEO0	MSEO1	**G**
VDDEH 10	GPIO 203	GPIO 204	SINB	**H**
SOUTB	PCSB3	PCSB0	PCSB1	**J**
PCSA3	PCSB4	SCKB	PCSB2	**K**
PCSB5	SOUTA	SINA	SCKA	**L**
PCSA1	PCSA0	PCSA2	VPP	**M**
PCSA4	TXDA	PCSA5	VFLASH	**N**
CNTXC	RXDA	RSTOUT	RSTCFG	**P**
WKPCFG	CNRXC	TXDB	RESET	**R**
RXDB	BOOTCFG1	PLLCFG2	VSSSYN	**T**
VDDEH 6	PLLCFG1	BOOTCFG0	EXTAL	**U**
VDD	VRCCTL	PLLCFG0	XTAL	**V**
VSUP	VDD	VRC33	VDDSYN	**W**
NC	VSS	VDD	VDD33	**Y**
VDDE5	CLKOUT	VSS	VDD	**AA**
CNRXB	VDDE5	ENGCLK	VSS	**AB**
19	**20**	**21**	**22**	