MPC5534EVB

Development Board for the Freescale MPC5534

OPTIONS and CONNECTIONS

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Cautionary Notes

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a) This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of CE and the FCC as a **CLASS A** product.

b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

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d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

Terminology

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be idled by installing on 1 pin so they will not be lost.

This development board applies hardwired option selections (VRL_EN and CUTAWAY 1 – 16). These option selections apply a circuit trace between the option pads to complete a default connection. This type connection places an equivalent Jumper Installed type option. The circuit trace between the option pads maybe cut with a razor blade or similar type knife to isolate the default connection provided. Applying the default connection again can be performed by installing the option post pins and shunt jumper, or by applying a wire between the option pads.

MPC5534EVB Getting Started

The MPC5534EVB is provided in a kit with basic cables, power supply, support CD, and 3rd party software demonstration tools if provided. The support CD contains drawings, manuals, data sheets, and Freescale support software. Software development for the MPC5534 is supported by the Nexus debug port interface to a host PC operating a development tool suite for the MPC5500 devices. Several vendors provide tool suites and these must be purchased or licensed separately. Users should be experienced in embedded applications to apply this product.

MPC5534EVB Configuration

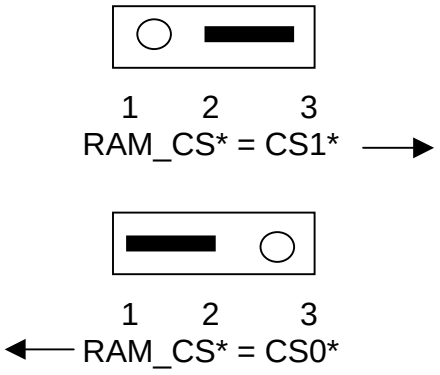
CONFIG Switch

The CONFIG switch provides reset configuration options for the MPC5534 device. Configuration options are enabled by position 1 of the switch. Switch positions 2 – 6 OFF provide an active low output condition to the respective configuration signal. Switch position ON will provide an active high signal condition.

POSITION	CONFIGURATION SIGNAL	DESCRIPTION
6	WKPCFG	**ON = default**, Refer to Freescale MPC5534 Documentation
5	PLLCFG1	**OFF = default**, Refer to Freescale MPC5534 Documentation
4	PLLCFG0	**ON = default**, Refer to Freescale MPC5534 Documentation
3	BOOTCFG1	**OFF = default**, Refer to Freescale MPC5534 Documentation
2	BOOTCFG0	**ON = default**, Refer to Freescale MPC5534 Documentation
1	CONFIG enable	**OFF= default.** ON = enables the RCON configuration to be applied from the switch settings.

SRAM_SEL Option

The MPC5534EVB board provides a 256K x 18 synchronous SRAM (U2) on the 16 bit data bus D0 – D15. SRAM data bits 16 and 17 are not applied. SRAM_SEL provides selection of the CS0 or CS1 chip selects to access the external SRAM (U2) on the EVB board. Chip select configuration should be set for 0 wait states, 512K byte memory range, WE signals = Write Enable. The SRAM supports 4 word BURST mode access also.



POWER Supply

This section covers the MPC5534EVB board power supplies and options. The primary power supply is the MC33730 device configured to support the MPC5534 device. The MPC5534 VRC regulator provides the VDD (1.5V) supply in the default configuration (CT1 and CT4 Open, CT2 and CT3 closed). MC33730 1.5V supply may be applied by optional configuration to provide the VDD 1.5V supply (CT1 and CT4 closed, CT2 and CT3 open).

Power supply Reset signals for the 5V, 1.5V and 3.3V supplies are applied to the MPC5534 RESET* input by the closed S1 – S3 option pads respectfully. The open S0 option pad may apply the RSTKAM* back-up supply reset signal if closed by the user. Also see the POWER_PORT connection and MC33730 data sheet for power supply access details.

ON_OFF Switch

The ON_OFF toggle switch provides ignition on and off control to the MC33730 supply. The MC33730 device will enable and disable the main power supplies. With the switch in the ON position, all power indicators should light. Inspect input power connection and source, and fuse F1 if power indication does not occur.

PWR - Power Jack

The Power Jack provides the default power input to the board. The jack accepts a standard 2.0 ~ 2.1mm center barrel plug connector (positive voltage center) to provide the +VIN supply of +6 to +24 VDC (+12VDC typical).

+Volts, 2mm center

FUSE – F1

Input power is limited by fuse F1. A 5x20mm type 1A slow-blow type fuse is applied to protect the EVB board for overload conditions.

POWER Port

Power Port provides access to the main power supplies and MC33730 optional supplies. Note that the +VIN connection provided at pin 1 is not switched by the ON-OFF switch or fused and is directly connected to the Power Jack.

PIN #		SIGNAL DESCRIPTION
1	2	+V IN= DC input voltage from PWR jack (NO fuse or polarity protection).
3	4	+5V = regulated +5V supply from MC33730
5	6	+3.3V = regulated +3.3V supply from MC33730
7	8	+1.5V = regulated +1.5V supply from MC33730
9	10	VDD = MPC5534 VDD supply, 1.5V typically
11		VREF1 = MC33730 Optional 5V reference supply.
	12	+5VA = MC33730 VREF2 output dedicated to the MPC5534 5V analog supply.
13		RST3* = 3.3V power supply reset signal from MC33730 supply.
	14	VSTBY = 1V backup / standby voltage applied to MPC5534 VSTBY input. See VSTBY_SW and CT9 option also.
15		RSTL* = 1.5V power supply reset signal from MC33730 supply.
	16	REGON = control signal to the M33730, see MC33730 user guide.
17		RSTH* = 5V power supply reset signal from MC33730 supply.
	18	IGN_ON = control signal output from the MC33730, see MC33730 user guide.
19		RSTKAM* = Keep Alive / VSTBY / backup power supply reset signal from the MC33730.
	20	PFD = control signal output from the MC33730, see MC33730 user guide.
21	22	Ground / VSS

VSTBY SWITCH and CT9

The VSTBY SWITCH provides enabling and disabling the VSTBY operation of the MPC5534 internal RAM. Switch in the OFF position disables the VSTBY operation and the VSTBY pin is connected to VSS / Ground. Switch in the ON position applies the +1VDC VKAM standby voltage from the MC33730 supply to the VSTBY pin.

Cut-away option CT9 allows the user to isolate the VSTBY pin of the MPC5554 from the switch. With CT9 open, the user must apply external battery or ground to the VSTBY position on the Power Port connector or I/O header ring.

ANALOG Supplies

The MPC5554 VDDA supply (+5V default) is provided by the MC33730 VREF2 regulator output. VRH reference supply is provided by VDDA by default with the VRH_EN option jumper installed. External VRH reference may be applied by removing the VRH_EN option and applying reference voltage at header ring I/O pin A10. The VRL_EN closed option pads connect the signal to common VSS supply by default. User may open this option to apply a precision ground to the VRL signal.

The QADC digital supply is provided +5V by option CT8. An optional connection to +3.3V for the QADC is provided by CT7. CT8 must be opened to install CT7 for +3.3V operation. See the MPC5534 user manual for more details on operating the QADC at +3.3V and limitations of the VDDA and VRH supplies.

USER Components

The EVB board provides an External clock option (X1), 8 LED indicators, an 8 position DIP switch, 4 push switches, a speaker with amplifier, and 2 user potentiometers. These devices are accessed via the USER LED, USER SWITCH, and USER DEV I/O headers. EVB board user may apply the devices to the MPC5534 I/O header signals to evaluate operation or assist in code development.

X1 CLOCK Oscillator

The X1 socket is provided to install standard 5V compatible CAN type clock oscillators so that alternate clock source or frequencies maybe applied to the MPC5534. User should refer to the MPC5534 device user manual for information on frequency selection and clocking configuration.

X1 clock signal is provided to the MPC5534 by option pad set CT6 being closed by 0 ohm resistor or mod wire application. CUT-AWAY option CT5 must be opened to remove the Y1 crystal from the EXTAL signal or problems may occur with operation. User should review the MPC5534 user guide for proper PLLCFG0 and PLLCFG1 (CONFIG Switch 4 and 5) option settings if an external clock is applied.

USER LED

User LED connector provides access to the user LED 1 to 8. Connector pins 1 to 8 are organized in a one to one connection to the individual indicators LED 1 to 8. The LED indicators are buffered for minimal drive current requirement (~300ua). Indicators will turn on with a logic high signal level of 2.5 to 5V applied at the respective connector pin.

USER Switch

User Switch provides access to the 8 position User DIP Switch. Connector pins 1 to 8 organization provide a one to one organization to the individual DIP switch positions 1 to 8. The switch connections are pulled low with 10K ohm resistors when the switch position in the off position. Switch positions placed in the ON position will provide a 3.3V output to the connector.

USER_DEV

User DEV provides access to the 4 push switches (SW1 – SW4), Speaker, and 2 user potentiometers (RV1 and RV2).

PIN #	USER COMPONENT CONNECTION
1	SW1 out, de-bounced CMOS drive 0 or 3.3V, active low.
2	SW1 out, de-bounced Open Drain output, active low, 10K ohm pull-up to 3.3V. Suitable for IRQ input signal drive.
3	SW2 out, active low, 10K ohm pull-up to 3.3V.
4	SW3 out, active low, 10K ohm pull-up to 3.3V.
5	SW4 out, active low, 10K ohm pull-up to 3.3V.
6	SPEAKER amp input. 0 to 5Vpp, volume adjust with SPKR_VOL.
7	RV1 center tap, 0 – 5V adjustment
8	RV2 center tap, 0 – 5V adjustment

SW1 – SW4 Push Switches

The push switches provide momentary active low input for user applications. SW1 has additional features of being de-bounced for no glitch operation and push-pull output on pin 1 or open drain output on pin 2. Typical user application would be to provide program control or menu selection input.

SW3_UP and SW4_Down are also provided for the UNI_3 Port motor control operation when the MOTOR_EN option is installed.

RV1 and RV2 User Potentiometers

The User Potentiometers provide an adjustable linear voltage output from 0 to 5V. The voltage signal may be applied to an MPC5534 analog input port for user application.

SPEAKER and SPKR_VOL

The speaker and amplifier provide user applications with a method to generate sound effects from a MPC5534 output. Frequency range of the amplifier input is 300Hz to 10Khz. The SPKR_VOL potentiometer allows user adjustment of the sound effect volume from the speaker. The amplifier also provides a SHDN input connection pad. This pad maybe connected to a MPC5534 output signal to disable the amplifier with a logic high signal of 3.3V or 5V.

MPC5534EVB I/O Ports

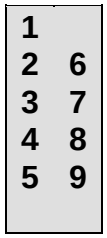
COM-1 Port

COM-1 is a standard RS232 type serial port configured for direct connection to a PC COM Port with a straight through type 9 pin serial cable. Option JP2 provides MPC5534 SCI channel 'A' signal connections when installed. Optional RTS and CTS hardware flow control connection pads are provided for the user to apply MPC5534 I/O ports and software to enhance operation.

JP2 Option

The JP2 Option provides MPC5534 RXDA and TXDA signals to the COM1 transceiver connections. This allows the user to apply the provided communication transceiver with the SCI A channel or to apply the associated I/O to other purposes. JP2 position 1 installed enables the TXDA output and position 2 enables the RXDA input on COM-1.

COM1



The **COM-1** port is a Female (socket type) DB9 connector.

Pins 1, 4, and 6 connected for status null to host.

Pins 7 and 8 maybe applied by CTS and RTS pads to MPC5534 I/O.

RTS signal active output level is logic 0. User should place I/O port applied at logic low (0) to enable the RTS signal and reception of bytes if applied. User should apply a logic high signal under software control inform host or connected RS232 device to STOP transmitting (stop sending incoming bytes).

CTS signal active input level is logic 0. User should apply software to detect a logic high signal or rising edge on applied I/O port and STOP transmitting bytes to the host or connected device to implement hardware flow control. Detection of a logic low input indicates the host is ready to receive bytes and the user may transmit.

DB9 connector pin locations are provided access pads behind the connector on the EVB board. User may isolate the connection pads by cutting the associated circuit trace on the bottom of the board.

CAN Port

The CAN Port provides 9 pin connector with a TJA1050 CAN transceiver interface to the MPC5534 CAN channels. The CAN_SEL option locations select the CAN channel applied to the transceiver and CAN Port. User may apply more than one MPC5534 CAN channel to the port if the open drain TX output type is applied on the associated CAN channel transmit pins.

CAN_SEL Option

The CAN_SEL option header allows selection of the MPC5534 CAN channels applied to the Power Oak transceiver and CAN Port. If more that one transmit channel is applied, transmit pins must apply the open drain output feature.

POSITION #	MPC5534 CAN SIGNAL
1	CNTX_A, channel A TX out (**DEFAULT enabled**)
2	CNRX_A, channel A RX in (**DEFAULT enabled**)
3	CNTX_B, channel B TX out (N/A with MPC5534)
4	CNRX_B, channel B RX in (N/A with MPC5534)
5	CNTX_C, channel C TX out
6	CNRX_C, channel C RX in

Following is the DB9S connection reference.

CAN_PORT

1	**1**		X
CAN_LO	**2**	**6**	GND
GND	**3**	**7**	CAN_HI
4	**4**	**8**	8
5	**5**	**9**	9

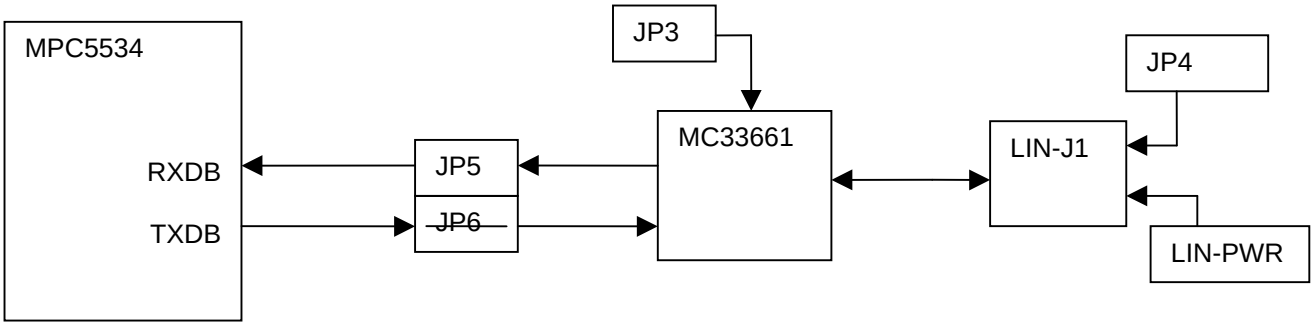
CAN port has a Female (socket type) DB9 connector.

CAN_HI and CAN_LO signals are terminated together with 120 ohms (R68).

DB9 connector pin locations are provided access pads behind the connector on the EVB board for additional user application.

LIN_J1

The LIN_J1 port provides a Master Mode LIN network connection. The MPC5534 device provides a LIN Master type node on the LIN Network. A LIN physical layer transceiver U7 (MC33661, or similar) is provided between the MPC5534 device and the LIN network connector. Refer to the MC33661 data sheet for complete details of transceiver operation. The following diagram represents the LIN connection:



The LIN interface provides optional features of slew rate control, network supply, and wake up option. See the JP3, JP4, JP5, JP6, LIN_PWR and CT10 options following.

CT10 Option

MPC5534 I/O signal GPIO203 provides LIN transceiver U7 enable control (EN pin). Software control of the EN pin allows the user to set the slew rate control of the transceiver. User applications should configure the GPIO203 pin for output to operate the LIN transceiver. If GPIO203 is needed for other purposes, the CT10 option maybe cut to isolate the signal from the LIN transceiver and JP3 installed to provide an enable to the transceiver. Refer to the MC33361 data sheet for further details of operation.

JP3 Option

Installation of JP3 applies a pull-up resistor on the LIN transceiver enable pin. MPC5534 GPIO203 may still control the transceiver enable operation when JP3 is installed.

JP5 Option

JP5 selects the MPC5534 SCI RXDB signal input to be from the LIN transceiver. For LIN operation JP5 must be installed.

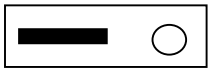
JP6 Option

JP6 is wired closed by default and not populated. JP6 provides the MPC5534 TXDB signal to the LIN transceiver. User may cut the JP6 wire trace to isolate the TXDB signal.

JP4 Option

LIN-J1 connector pin 2 may be configured for different network requirements by JP4. JP4 open will disconnect LIN-J1 pin 2 from the EVB board.

LIN-J1 pin 2 = Ground / VSS ⟶



⟵ LIN-J1 pin 2 = Transceiver WAKE pin

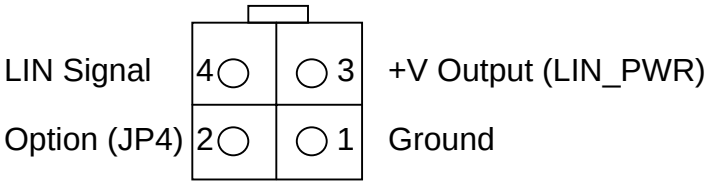
LIN_PWR Option

Installation of the LIN_PWR option applies MPC5534EVB +V input voltage (12V typical) for LIN network power to LIN-J1 pin 3. This connection allows the EVB board to operate as a LIN master node to power remote LIN slave nodes. User should use caution to not overload the F1 fuse and verify only one source is applied on the network.

LIN-J1 Connector

The LIN-J1 network connector provides a standard pin configuration with a network option position on pin 2.

Front view (looking into connector from outside of board edge)



Mating connector = Molex 39-01-2040 with 39-00-0039 pins.

TPU Port

The TPU_PORT provides an organized I/O port for the MPC5534 eTPU_A signals.

MPC5534 Signal	TPU Port		MPC5534 Signal
+3.3V	1	2	+5V
eTPU_A16	3	4	x
eTPU_A17	5	6	x
eTPU_A18	7	8	eTPU_A0
eTPU_A19	9	10	eTPU_A1
eTPU_A20	11	12	eTPU_A2
eTPU_A21	13	14	eTPU_A3
eTPU_A22	15	16	eTPU_A4
eTPU_A23	17	18	eTPU_A5
eTPU_A24	19	20	eTPU_A6
eTPU_A25	21	22	eTPU_A7
eTPU_A26	23	24	eTPU_A8
eTPU_A27	25	26	eTPU_A9
eTPU_A28	27	28	eTPU_A10
eTPU_A29	29	30	eTPU_A11
eTPU_A30	31	32	eTPU_A12
eTPU_A31	33	34	eTPU_A13
GND	35	36	eTPU_A14
TCRCLK_A	37	38	eTPU_A15
GND	39	40	GND

UNI_3 Motor Control Port

The UNI_3 Motor Control Port is provided for easy application of the Freescale UNI_3 Motor control application boards and motors. Many of the MPC5534 I/O signals are applied for the UNI_3 motor control application so the user should review I/O application carefully. UNI_3 port operation is enabled by the MOTOR_EN option jumper installation.

MOTOR_EN Option

This option controls the connection of the MPC5534 I/O ports to the UNI_3 and HALL_ENCODER motor control ports. When installed, signal buffers U13 and U15 are enabled to apply MPC5534 I/O for motor control.

UNI_3 Port

The UNI_3 port is the primary motor control I/O port for application of the UNI_3 motor control development boards. Following are the signal assignments:

MPC5534 Signal	UNI_3 Signal	UNI_3 Port		UNI_3 Signal	MPC5534 Signal
eTPU_A8	PWM_AT	1	2	Common 4,6,8,10	x
eTPU_A9	PWM_AB	3	4	Common 2,6,8,10	x
eTPU_A10	PWM_BT	5	6	Common 2,4,8,10	x
eTPU_A11	PWM_BB	7	8	Common 2,4,6,10	x
eTPU_A12	PWM_CT	9	10	Common 2,4,6,8	x
eTPU_A13	PWM_CB	11	12	GROUND	VSS / GROUND
VSS / GROUND	GROUND	13	14	x	
	x	15	16	x	
VSSA	ANALOG GND	17	18	ANALOG GND	VSSA
	x	19	20	x	
AN16	VS_DCB	21	22	IS_DCB	AN17
AN18	IS_A	23	24	ISB	AN19
AN20	IS_C	25	26	x	
	x	27	28	x	
eTPU_A15	BRAKE	29	30	x	
	x	31	32	x	
	x	33	34	ZX_A	eTPU_A5
eTPU_A6	ZX_B	35	36	ZX_C	eTPU_A7
	x	37	38	BEMF_A	AN21
AN22	BEMF_B	39	40	BEMF_C	AN23

HALL ENCODER Port

The Hall encoder port is provided for motor position feedback signals from the UNI_3 motor application development boards.

HALL Port	HALL Signal	MPC5534 Signal
1	+5V	+5V / VDDH
2	GROUND	VSS / GROUND
3	H_1	eTPU_A1
4	H_2	eTPU_A2
5	H_3	eTPU_A3
6	H_4	eTPU_A4
x	H_CLK	TCRCLK_A, H_CLK is derived by logic from the H_1 – 4 signals.

RUN STOP Switch

The RUN STOP switch is connected to the MPC5534 EMIOS11 signal pin. The switch provides a motor run or stop condition input for the motor control application.

RV4 FAULT Adjust and Fault Indicator

RV4 Fault Adjustment is provided to set the applied motor over-current fault condition. The IS_DCB current sense input from the UNI_3 port is compared by U16 with the RV4 setting to determine if an over-current condition exists. If the IS_DCB input signal is greater than the RV4 setting, the Fault condition becomes active. The FAULT indicator will light and an active low Fault signal will be provided to MPC5534 EMIOS10 signal pin.

SW3_UP and SW4_Down

User switches SW3 and SW4 provide the motor speed UP and DOWN input signals when the MOTOR_EN option is installed. Both switches are active low. SW3_UP signal is provided to the MPC5534 EMIOS8 signal pin. SW4_DOWN signal is provided to the MPC5534 EMIOS9 signal pin.

DEVELOPMENT PORTS

The MPC5534EVB board provides 1 JTAG and 2 NEXUS type development ports. Only one of the development ports should be applied due to common signals used on the ports. The development port input and power signals are buffered by a CBTLV3861 device. This buffer provides a bi-directional 5 ohms series resistance on the input signals when powered on. The buffer also provides signal isolation when powered off.

The EVB board applies 100ohm terminations (R89 and R90) on the CLKOUT signal to the Nexus ports. This termination is not recommended for other designs. The Nexus port should be placed as close as possible to the MPC5534 for best solution.

NOTE: Proper power sequencing must be performed when a development port is applied (cable connected). Development port application power sequence:

1) MPC5534EVB board ON–OFF switch is OFF and no power is applied to the PWR connector.

2) Connect development port cable to the desired MPC5534EVB board development port.

3) Apply power to the MPC5534EVB board PWR connector and turn ON–OFF switch ON.

4) If power is removed or the ON-OFF switch is turned off, remove development cable from board connector and re-apply from step 1 of this procedure.

JTAG Port

The JTAG port provides a Freescale standard JTAG connection to the MPC5534. The connector is a standard 2x7, .1 inch pin space keyed pin header. Example compatible cables include the OCDEMON™ NP-JTAG ONCE "Wiggler" and the P&E Microcomputer Systems CABPPCNEXUS. Host software must be applied to operate the cables.

JTAG Port

Signal	Pin #	Pin #	Signal
B_TDI	1	2	GND
TDO	3	4	GND
B-TCK	5	6	GND
B_EVTI*	7	8	JTG8 TP
B-RESET*	9	10	B_TMS
B_+3.3V	11	12	GND
B_RDY*	13	14	B_JCOMP

Notes:
1) B_… signals are buffered.
2) JTG8 TP signal is not connected to the MPC5534 and provides a Test Pad on the board.
3) Signals followed by a "*" symbol are active logic low.
4) Pin 7 or the B_EVTI* signal may not be supported by all development cables. Option CT11 cut will isolate this signal if not supported by the development cable and issues are present.

NEXUS Port

The NEXUS port provides a more powerful and higher speed development port for high end tools. The port connector is an AMP 38 pin Mictor style, part number #767053-1.

NEXUS Port

Signal	Pin #	Pin #	Signal
NXS1 TP	1	2	NXS2 TP
NXS3 TP	3	4	NXS4 TP
MDO9	5	6	CLKOUT
BOOTCFG1	7	8	MDO8
B_RESET*	9	10	B_EVTI*
TDO	11	12	B_+3.3V
MDO10	13	14	B_RDY*
B_TCK	15	16	MDO7
B_TMS	17	18	MDO6
B_TDI	19	20	MDO5
B_JCOMP	21	22	MDO4
MDO11	23	24	MDO3
ERSTOUT*	25	26	MDO2
NXS27 TP	27	28	MDO1
NXS29 TP (Note 3)	29	30	MDO0
+V	31	32	EVTO*
+V	33	34	MCKO
NXS35 TP (Note 3)	35	36	MSEO1*
B_VSTBY	37	38	MSEO0*

Notes:
1) B_… signals are buffered.
2) NXSxx TP signals are not connected to the MPC5534 and provide a Test Pad on the board.
3) NXSxx signal TP is also connected to the ROBUST Nexus connector.
4) Signals followed by a "*" symbol are active logic low.

ROBUST Nexus Port

The ROBUST port connector location is provided for user expansion. This port provides the ROBUST Nexus 51 pin location that applies the GLENAIR MR7580-51P2BNU connector.

ROBUST Port

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	+V	19	MDO0	36	GND
2	+V	20	GND	37	MDO4
3	B_VSTBY1	21	MCKO	38	GND
4	NXS35 TP	22	GND	39	MDO5
5	TDO	23	EVTO*	40	GND
6	B_RDY*	24	GND	41	MDO6
7	B_RESET*	25	MSEO0*	42	GND
8	B_+3.3V	26	MDO9	43	MDO7
9	B_EVTI*	27	MDO1	44	GND
10	GND	28	GND	45	MDO8
11	B_JCOMP	29	MDO2	46	GND
12	GND	30	GND	47	MDO10
13	B_TMS	31	MDO3	48	GND
14	GND	32	GND	49	MDO11
15	B_TDI	33	NXS29 TP	50	GND
16	GND	34	GND	51	JP1 pin 2
17	B_TCK	35	MSEO1*		
18	GND				

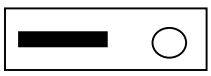
Notes:
1) NXS29 and NXS35 signals are also connected to the NEXUS connector.
2) Signals followed by a "*" symbol are active logic low.

JP1 Option

JP1 provides signal selection for the Robust Nexus connector pin 51. Position 1-2 provides the BOOTCFG1 signal and position 2-3 provides the ERSTOUT* signal.

1 2 3

Robust pin 51 = ERSTOUT* ⟶



1 2 3

⟵ Robust pin 51 = BOOTCFG1

MPC5534 I/O HEADER RING

MPC5534 I/O signals are provided by the I/O header ring. The header ring consists of .1 inch grid pins organized in 4 rows for each side of the MPC5534 device. Each row reflects the corresponding location of the MPC5534 device BGA package ball ring. Signals indicated are the EVB board primary function.

A1 – AB4 HEADER

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
A1	GND	A2	VDD	A3	VSTBY	A4	AN37
B1	3.3V	B2	GND	B3	VDD	B4	AN36
C1	eTPU_A30	C2	eTPU_A31	C3	GND	C4	VDD
D1	eTPU_A28	D2	eTPU_A29	D3	eTPU_A26	D4	GND
E1	eTPU_A24	E2	eTPU_A27	E3	eTPU_A25	E4	eTPU_A21
F1	eTPU_A23	F2	eTPU_A22	F3	eTPU_A17	F4	eTPU_A18
G1	eTPU_A20	G2	eTPU_A19	G3	eTPU_A14	G4	eTPU_A13
H1	eTPU_A16	H2	eTPU_A15	H3	eTPU_A10	H4	5V
J1	eTPU_A12	J2	eTPU_A11	J3	eTPU_A6	J4	eTPU_A9
K1	eTPU_A8	K2	eTPU_A7	K3	eTPU_A2	K4	eTPU_A5
L1	eTPU_A4	L2	eTPU_A3	L3	eTPU_A0	L4	eTPU_A1
M1	BDIP*	M2	TCRCLK_A	M3	CS1*	M4	CS0*
N1	CS3*	N2	CS2*	N3	WE1*	N4	WE0*
P1	A16	P2	A17	P3	RD_WR	P4	3.3V
R1	A18	R2	A19	R3	3.3V	R4	TA*
T1	A20	T2	A21	T3	A12	T4	TS*
U1	A22	U2	A23	U3	A13	U4	A14
V1	A24	V2	A25	V3	A15	V4	A31
W1	A26	W2	3.3V	W3	A30	W4	GND
Y1	A28	Y2	A27	Y3	GND	Y4	VDD
AA1	A29	AA2	GND	AA3	VDD	AA4	3.3V
AB1	GND	AB2	VDD	AB3	3.3V	AB4	D0

< See Errata below

A18 – D5 HEADER

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
A18	MDO10	B18	MDO7	C18	MDO2	D18	MDO3
A17	MDO11	B17	MDO9	C17	MDO5	D17	MDO6
A16	AN12	B16	AN13	C16	AN14	D16	AN15
A15	VSSA	B15	VSSA	C15	VDDA0	D15	VDDEH9
A14	AN35	B14	AN32	C14	AN33	D14	AN34
A13	AN28	B13	AN31	C13	AN30	D13	AN29
A12	AN27	B12	AN26	C12	AN25	D12	AN24
A11	VRL	B11	AN23	C11	AN22	D11	AN6
A10	VRH	B10	x	C10	AN7	D10	AN2
A9	AN5	B9	AN4	C9	AN3	D9	AN18
A8	AN1	B8	AN0	C8	AN21	D8	AN10
A7	VSSA	B7	AN16	C7	AN20	D7	AN9
A6	VDDA1	B6	AN19	C6	AN17	D6	AN38
A5	AN11	B5	AN39	C5	AN8	D5	VDD

A19– AB22 HEADER

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
A19	MDO8	A20	VDD	A21	3.3V	A22	GND
B19	MDO4	B20	MDO0	B21	GND	B22	3.3V
C19	MDO1	C20	GND	C21	3.3V	C22	VDD
D19	GND	D20	3.3V	D21	TCK	D22	TDI
E19	3.3V	E20	TMS	E21	TDO	E22	TEST*
F19	3.3v	F20	JCOMP	F21	MSEO0*	F22	EVTO*
G19	RDY*	G20	MCKO	G21	EVTI*	G22	MSEO1*
H19	5V	H20	GPIO203	H21	GPIO204	H22	SIN_B
J19	SOUT_B	J20	PCS_B3	J21	PCS_B0	J22	PCS_B1
K19	PCS_A3	K20	PCS_B4	K21	SCK_B	K22	PCS_B2
L19	PCS_B5	L20	SOUT_A	L21	SIN_A	L22	SCK_A
M19	PCS_A1	M20	PCS_A0	M21	PCS_A2	M22	5V
N19	PCS_A4	N20	TXDA	N21	PCS_A5	N22	3.3V
P19	CNTX_C	P20	RXDA	P21	RSTOUT*	P22	RSTCFG*
R19	WKPCFG	R20	CNRX_C	R21	TXDB	R22	RESET*
T19	RXDB	T20	BOOTCFG1	T21	GND	T22	VSSSYN
U19	5V	U20	PLLCFG1	U21	BOOTCFG0	U22	x (EXTAL)
V19	VDD	V20	x (VRCCTL)	V21	PLLCFG0	V22	x (XTAL)
W19	GND	W20	VDD	W21	VRC33	W22	VDDSYN
Y19	x (NC2)	Y20	GND	Y21	VDD	Y22	3.3V
AA19	3.3V	AA20	CLKOUT	AA21	GND	AA22	VDD
AB19	CANRX_B	AB20	3.3V	AB21	ENGCLK	AB22	GND

W18– AB18 HEADER

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
W18	x (NC1)	Y18	3.3V	AA18	CNRX_A	AB18	CANTX_B
W17	3.3V	Y17	CNTX_A	AA17	EMIOS23	AB17	EMIOS20
W16	EMIOS21	Y16	EMIOS22	AA16	EMIOS19	AB16	EMIOS18
W15	EMIOS12	Y15	EMIOS17	AA15	EMIOS16	AB15	EMIOS14
W14	5V	Y14	EMIOS15	AA14	EMIOS13	AB14	EMIOS11
W13	EMIOS8	Y13	EMIOS10	AA13	EMIOS9	AB13	EMIOS7
W12	EMIOS2	Y12	EMIOS6	AA12	EMIOS5	AB12	EMIOS4
W11	D14	Y11	D15	AA11	EMIOS3	AB11	EMOS1
W10	D12	Y10	D13	AA10	3.3V	AB10	EMOS0
W9	D11	Y9	GPIO207	AA9	D7	AB9	OE*
W8	3.3V	Y8	D10	AA8	D5	AB8	D6
W7	3.3V	Y7	D9	AA7	GPIO206	AA7	D4
W6	3.3V	Y6	D8	AA6	3.3V	AA6	D3
W5	VDD	Y5	3.3V	AA5	D1	AA5	D2

Note: Indicated as W18 / AB6 on EVB board.

EVB HEADER ERRATA

EVB revisions A, B, and C incorrectly connect I/O header pins F3 and F4. MPC5534 pin F3 signal eTPU_A17 appears on header pin F4. MPC5534 pin F4 signal eTPU_A18 appears on header pin F3. This error is corrected on revision D and later.