M52235EVB

Development Board for Freescale MCF5223x MCU
Hardware User Manual

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Cautionary Notes

1) Electrostatic Discharge (ESD) prevention measures should be applied whenever handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing reserves the right to make changes without further notice to any products to improve reliability, function or design. Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the M52235EVB board:

   a) This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
      1) This device may not cause harmful interference, and
      2) This device must accept any interference received, including interference that may cause undesired operation.

   b) This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of CE IT Equipment **CLASS A** product.

   c) This product is designed and intended for use as a development platform for hardware or software in an educational / professional laboratory.

   d) In a domestic environment this product may cause radio interference in which case the user may be required to take adequate prevention measures.

Terminology

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

> Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.
>
> Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

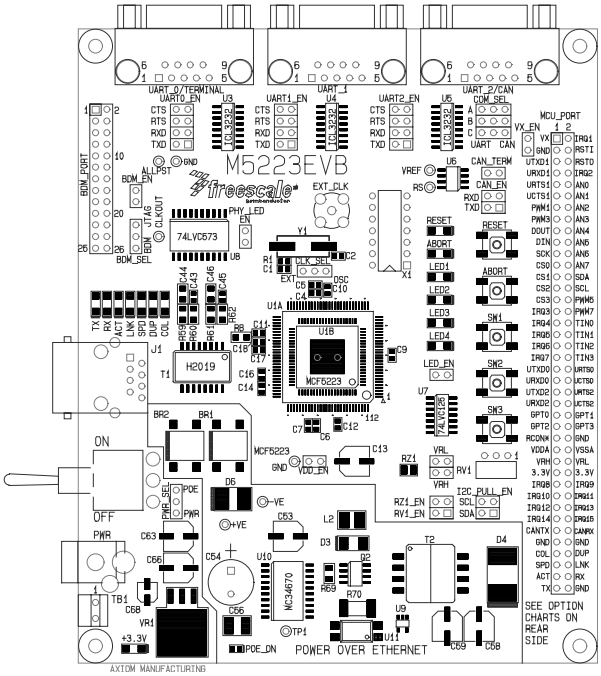
Signal names in this document that are followed by an asterisk (*) denote an active-low signal.

FEATURES

M52235EVB is a low cost development system for the Freescale MCF5223x ColdFire® microcontroller. Application development is quick and easy with the included DB9 serial cable and dBUG firmware monitor. The BDM port is compatible with standard ColdFire BDM / JTAG interface cables and hosting software, allowing easy application debugging and development with a variety of hardware and software tools.

Features:

- MCF52235 CPU, 112 pin LQFP
  - * 256K Byte Flash (on-chip)
  - * 32K Byte SRAM (on-chip)
  - * Integrated 10/100 FEC+EPHY
  - * DMA Controller w/ four 32-bit Timers
  - * Interrupt Controller
  - * Cryptographic Accelerator Unit (CAU)
  - * 8 Channel 12-bit A/D
  - * QSPI, IIC, and CAN Serial Ports
  - * 3 UART Serial Ports with DMA capability
  - * Edge / Interrupt Port
  - * 8 PWM timers
  - * 4 16-bit GPT Timers
  - * BDM / JTAG Port
  - * Internal Oscillator w/ PLL clock
  - * 3.3V operation
- 25MHz reference crystal
- MCU port, 80 pin I/O port
- BDM / JTAG Port, 26-pin development port
- UART0 / Terminal Port w/ RS232 DB9-S Connector
- UART1 Port w/ RS232 DB9-S Connector
- UART2 / CAN port w/ RS232 and 1Mbaud CAN transceiver
- 10/100TX Port with POE power supply
- RESET switch and indicator
- ABORT (IRQ7) switch
- 4 User and 7 10/100TX Status Indicators (LED)
- 3 User Push Switches
- Regulated +3.3V power supply w/ indicator
- Supplied with DB9 Serial Cable, 10/100 Ethernet cable, Wall Adapter Power supply, and P&E BDM interface cable.



M52235EVB

Specifications:
Board Size 4.5” x 5.5”
Power Input: +5 - +25VDC, 9VDC typical
POE supply Input: 48V typical
Current Consumption: 150ma typical @ 9VDC input

The M52235EVB is provided operating a firmware application. Refer to the M52235EVB Quick Start Guide for more information on operation. The EVB kit is plug in and play out of the box with a wall adapter power supply, cables, support CD, and example software. Additional hardware and software development tools are available, but not required.

GETTING STARTED

The M52235EVB single board computer is a fully assembled, fully functional development board for the Freescale MCF5223x microcontrollers. It is provided with a wall plug power supply, 10/100TX Ethernet cable, P&E BDM interface cable, and a serial cable. Provided support software for this development board is for Windows 95/98/NT/2000/XP operating systems.

Development board users should also be familiar with the hardware and software operation of the target MCF52235 device. Refer to the microcontroller reference manual, MCF5223xRM, for details. The purpose of the development board is to assist the user in quickly developing an application with a known working environment, to provide an evaluation platform. Users should be familiar with memory mapping, memory types, and embedded software design for the quickest successful application development.

Software Development

Application development may be performed by applying a firmware debug monitor, or by applying a compatible ColdFire BDM / JTAG cable with supporting host software. The CFFlasher Programming software is provided for updating the contents of the MCF52235 flash memory.

Software development is best performed with a development tool connected to the BDM port. This provides real-time access to all hardware, peripherals and memory on the board. Development tool software also provides high-level (C/C++) source code debug environment.

The target development environment and procedure for best success is to place software to be tested into RAM memory. Execute software to be tested under a firmware monitor or development tool control. If applying a firmware monitor, port the code to replace the monitor in the flash memory and update with the CFFlasher software. Many application notes, example software, and supporting tools can be located on the www.freescale.com/coldfire or device product web pages.

Reference Documentation

The following documents should be referenced when developing with the M52235EVB. These documents are available on the MCF52235 and M52235EVB web pages (http://www.freescale.com/coldfire).

M52235EVBUM – This user manual.
MCF52235RM – MCF52235 Device Reference Manual
CFPRM – ColdFire Programmers Reference Manual with instruction set
M52235EVB_SCH_D – M52235EVB board schematics

M52235EVB Startup

Follow these steps to connect and power on the board for the default dBUG monitor operation.

1) Carefully unpack the M52235EVB and observe ESD preventive measures while handling the M52235EVB development board.

2) Review option settings on the EVB. Most options are provided with default setting information on the bottom side of the EVB.

3) Review the support CD and copy documentation or install software as wanted. Refer to the Quickstart document if provided and apply the instructions.

4) Connect necessary cables between host PC and EVB board prior to applying power to the EVB.

5) Apply power to the development board by installing the wall plug power supply between a wall outlet and the PWR Jack on the board. Set the ON / OFF switch to the ON position. The EVB +3.3V voltage indicator should turn on at this time. Note: PWR_SEL = PWR setting, see the POE section for operating the POE supply.

6) Review the Quickstart for preloaded application operation or launch development tools.

7) The board is ready to use now. See the Quickstart document or development tools user manuals for additional information. If BDM / JTAG development port interfaced tools are to be applied, see the BDM PORT section of this manual for more details on cable installation.

M52235EVB Hardware Configuration and Options

The M52235EVB board provides a basic development or evaluation platform for the MCF5223x microcontrollers. Following are descriptions of the main components and options provided on the board.

MEMORY

The EVB memory is the internal MCF52235 device SRAM and Flash memory. The MCF52235 provides 32K bytes of SRAM and 256K bytes of Flash memory internally. Refer to the device user guide for memory details. If a dBUG monitor is applied, refer to the monitor user guide for memory map information.

POWER SUPPLIES

The EVB provides two regulated power supplies, standard DC regulator (PWR) and the Power Over Ethernet (POE) regulator. Both power supplies may be powered on at the same time but only one may be applied to power the EVB board. The PWR_SEL option jumper selects which power supply will operate the EVB board. Default application is for unregulated low voltage DC to be applied by external connection to the Power Jack or TB1 terminal block. ON _OFF switch controls the 3.3V supply to the EVB.

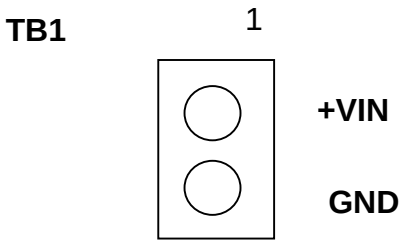
Power Jack (PWR)

The Power Jack provides the default power input to the board. The jack accepts a standard 2.0 ~ 2.1mm center barrel plug connector (positive voltage center) to provide the +VIN supply of +5 to +25 VDC (+9VDC typical).

+Volts, 2mm center

TB1 Power connection

TB1 terminal block provides access to the +VIN and GND (power ground) supplies. The +VIN supply should be limited to the range of +5 to +25 VDC (+9VDC typical).



Power Over Ethernet (POE) Supply

The POE supply (Freescale MC34670) input is from the J1 Ethernet connector. A POE enabled Ethernet switch or host equipment provides the supply for this input. The POE_ON indicator will be ON if this supply is available. This is an isolated type supply, test pads +VE and –VE must not be grounded by test equipment or damage may occur.

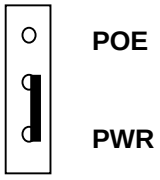
POE_ON Indicator

The POE_ON indicator will light if the Ethernet POE supply is powered and operating.

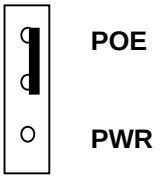
PWR_SEL Option

PWR_SEL option jumper provides selection of the PWR regulator, POE regulator, or +VX_EN external +3.3V input to power the EVB board. Default position is for PWR jack and regulator to provide power.

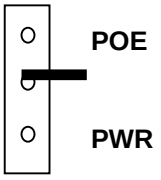
PWR_SEL = PWR



PWR_SEL = POE



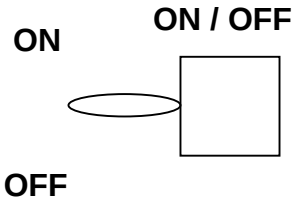
PWR_SEL = VX_EN



VX_EN = External 3.3V provided on pin 1 of MCU Port. PWR or POE supply 3.3V may be provided out to pin 1 of MCU port also if no external supply is provided at pin 1.

ON_OFF Switch

The ON_OFF switch provides power On and Off control for the 3.3V regulated voltage from the power supply selected by the PWR_SEL option.



+3.3V PWR Indicator

The +3.3V indicator will be ON if a 3.3V supply is available and the ON-OFF switch is ON.

VDD_EN Option

VDD_EN allows the user to isolate the MCF52235 device VDD pins to make measurements or provide an alternate supply. This option is installed by default. Do not operate the EVB without the proper power supplied to the MCF52235 supply pins.

VX_EN Option

The VX_EN option is provided to support external 3.3V input from the MCU PORT pin 1 in conjunction with Freescale educational accessories. The VX_EN option installed provides external 3.3V input (or output if wanted) on MCU Port pin1.

See the PWR_SEL Option section above to disable the on-board regulators.

RESET

External reset is provided by the RESET switch or user applied connection to the RSTI* signal on the MCU PORT pin 6. If the 3.3V supply to the MCF52235 is below operating level, the device internal voltage detector will cause the MCF52235 to stay in the RESET condition.

Application of RESET will cause the dBUG monitor or user application to initialize the MCF52235. The previous operating state of the MCF52235 will be lost.

RESET Switch

RESET switch provides for manual application of the MCF52235 RSTI* signal.

RESET Indicator

RESET indicator will be ON for the duration of a valid RSTO* signal. This operation indicates the MCF52235 is in the Reset state.

ABORT Switch

The ABORT switch provides for manual application of the IRQ7 interrupt signal. This operation will allow the dBUG monitor to stop execution of a user program and maintain the CPU operating state for user examination.

SW1 – SW3 User Switches

User switches 1 - 3 are available for application as needed. The switches provide an active low signal when pressed. SW1 applies the MCF52235 IRQ4 signal, SW2 applies the IRQ11 signal and SW3 applies the IRQ1 signal.

LED[4:1] User Indicators

Four user indicators are provided for application on the MCF52235 DTIN[3:0] signals (configurable as GPIO). Indicators are buffered so they do not load the MCF52235 I/O ports. The LED_EN option will enable the LED buffer.

Indicator Table

INDICATOR	COLOR	OPERATION	DEFAULT CONDITION
LED1	Green	MCF52235 DTIN0 status, high = ON	ON
LED2	Green	MCF52235 DTIN1 status, high = ON	ON
LED3	Green	MCF52235 DTIN2 status, high = ON	ON
LED4	Green	MCF52235 DTIN3 status, high = ON	ON

LED_EN option

The user LED indicators LED[4:1] must be enabled by the LED_EN option installed.

RV1 and RV1_EN

User potentiometer RV1 provides a 0 – 3.3V level to MCF52235 ADC channel AN0 when RV1_EN option is installed on both pins. Adjusting RV1 turn knob will vary the voltage level. To apply the MCF52235 AN0 to an external signal, RV1_EN should be open / idle.

RZ1 and RZ1_EN

Visible light sensor RZ1 provides a 0.3 – 3.3V level to MCF52235 ADC channel AN1 when RZ1_EN option is installed on both pins. RZ1 will reduce the voltage level in respect to an increase in visible light on the sensor. To apply the MCF52235 AN1 to an external signal, RZ1_EN should be open / idle.

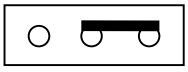
SYSTEM CLOCK

The EVB provides a 25MHz crystal oscillator reference input in Pierce Mode configuration. The MCF52235 also provides an internal relaxation oscillator. The not populated EXT_CLK SMA connector position and X1 clock position are available for the user to apply external clocks if wanted. The X1 position will allow a 3.3V standard or half size CAN type clock oscillator to be installed in the pin 1 aligned position. The CLK_SEL option provides the clock source selection.

CLK_SEL Option

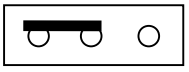
CLK_SEL provides selection of the EVB crystal oscillator Y1 or an External Clock source from EXT_ CLK or X1 as the primary input clock to the MCF52235 device.

CLK_SEL = Y1 crystal (Default)



EXT OSC

CLK_SEL = EXT (X1 or EXT_CLK)



EXT OSC

UART0_TERMINAL and UART1 Ports

The UART0_TERMINAL port provides the primary interface to the dBUG monitor with a default baud rate of 19.2K baud, 8 data bits, 1 stop bit, and no parity. Both the UART0 and UART1 ports apply a standard 9-pin serial connector with RS232 type interface to the MCF52235 UART0 or UART1 serial ports. Both ports apply a UARTx_EN option jumper block to enable the MCF52235 UART signals to operate the RS232 ports. A straight through DB9 Male / Female type serial cable can be applied to connect the ports to a standard PC COM port. Following is the DB9S connection reference.

UART0_TERMINAL and UART1 Ports

1	**1**		X	DB9 socket connector with RS232 signal levels. **1,4,6 connected for status null to host**
TXD	**2**	**6**	6	
RXD	**3**	**7**	7 CTS	
4	**4**	**8**	8 RTS	
GND	**5**	**9**	9	

UART0_EN and UART1_EN Options

OPTION Name	UART0_EN MCF52235 signal applied	UART1_EN MCF52235 signal applied
TX	UTXD0 output	UTXD1 output
RX	URXD0 input	URXD1 input
RTS	URTS0* output	URTS1* output
CTS	UCTS0* input	UCTS1* input

UART2_CAN Port

The UART2_CAN port provides the UART2 RS232 serial port or the CAN network port. Selection of the port interface type is provided by the COM_SEL option jumper block. Additional options provide MCF52235 signal connection to the selected interface transceiver for the port. The UART2_EN option block enables the MCF52235 UART2 signals for RS232 operation and the CAN_EN option block enables the MCF52235 CAN signals for CAN network operation. The CAN port also has a network termination option, CAN_TERM and biasing components RCAN1 and RCAN2 (not populated).

A straight through DB9 Male / Female type serial cable can be applied to connect the UART2 port in RS232 COM mode to a standard PC COM port. CAN mode connection will require the cabling to be compatible to the network applied. Following is the DB9S connection reference:

UART2_CAN Port

CAN	RS232	DB9		RS232	CAN	DB9 socket connector.
4, 6 tie	4, 6 tie	**1**			CAN Signal	**1,4,6 connected for RS232 status null to host**
CAN_LO	TXD	**2**	**6**	1, 4 tie	1, 4 tie	
GND	RXD	**3**	**7**	7 CTS	CAN_HI	
1, 6 tie	1, 6 tie	**4**	**8**	8 RTS	Do not connect	
GND	GND	**5**	**9**	X		

COM_SEL Option

Selects UART2_CAN Port connector type of interface between UART2 RS232 operation and CAN operation. All 3 positions should be set for the same selection, UART or CAN.

COM_SEL

Position	UART option	DB9 Connection	CAN Option
A	CTS	Pin 7	CAN_HI
B	RXD	Pin 3	GND
C	TXD	Pin 2	CAN_LO

UART2_EN option

UART2_EN applies the MCF52235 UART2 signals to the UART2 RS232 level transceiver for operation on the UART2_CAN connector.

OPTION Name	UART2_EN MCF52235 signal applied
TX	UTXD2 output
RX	URXD2 input
RTS	URTS2* output
CTS	UCTS2* input

CAN Operation

The MCF52235 FlexCAN signals CANRX and CANTX are the secondary operation of the MCF52235 SYNCA and SYNCB signals. User must enable the CAN signal operation on the MCF52235 I/O port during the FlexCAN initialization. The FlexCAN transmit and receive signals are connected to the CAN transceiver with the CAN_EN option block. To apply SYNC functions on these signals the CAN_EN options must be open or idle.

The CAN port provides the physical interface layer for the MCF52235 FlexCAN Controller Area Network version 2.0B peripheral. The FlexCAN transmit and receive signals are connected to a 3.3V CAN transceiver capable of 1M baud communication (SN65HVD230) with the CAN_EN option block. Transceiver differential CAN network signals (CAN_HI and CAN_LO) are provided to the COM_SEL option block for connection by the UART2_CAN port connector.

The CAN transceiver has CAN signal drive control via the **RS** test pad on the development board. The RS signal is provided a 1K Ohm pull-down resistor for the maximum signal rate setting. User may refer to the SN65HVD230 data sheet and apply additional transmit signal control at the RS test pad.

Bias options RCAN1 and RCAN2 (SMT 0805 size, not populated) provide idle bias connections for the CAN network if required by the user.

CAN_TERM

Installs a 62 ohm termination between the CAN_HI and CAN LO signals. Each end of a CAN network must be terminated for proper operation.

CAN_EN option

Enable MCF52235 CAN signals to the CAN transceiver with this option.

Position	MCF52235 Signal
TXD	CANTX / SYNCA
RXD	CANRX / SYNCB

J1 Ethernet Port

J1 (RJ45 type) provides the 10/100TX Ethernet physical interface connection and the Power Over Ethernet (POE) supply input. Port configuration applies the MCF52235 Fast Ethernet controller (FEC) and Embedded Physical Layer Interface (EPHY). The coupling transformer T1 provides port isolation and power path to the POE supply. MCF52235 PHY operation provides 7 status indicators under software control that may be enabled by the PHY LED EN option.

PHY LED ENable

This option jumper enables the PHY status indicator buffer so that the PHY status / indicator port controls the indicators. The indicators may also be applied as MCF52235 General Purpose indications if EPHY status use is not desired. The indicators are Active Low Level.

Ethernet PHY Status Indicators

Indicator	Color	MCF52235 Signal	EPHY Status (software configured)
TX	Green	TX_LED	Transmitting data
RX	Green	RX_LED	Receiving data
ACT	Green	ACT_LED	Active – Transmitting or Receiving
LNK	Green	LNK_LED	Link is detected
SPD	Green	SPD_LED	ON = 100T, OFF = 10T
DUP	Green	DUP_LED	ON = Full duplex, OFF = half
COL	RED	COL_LED	ON = 10T mode packet collisions

Note: Ethernet port must be initialized and operating for status indications.

Refer to the M52235EVB_SCH_D.pdf drawing for details on hardware connections to this port.

I2C Pull Enable

This option jumper block provides 1K ohm pull-ups to +3.3V for the MCF52235 I2C serial port signals SDA and SCL. These signals must be pulled up for the I2C serial bus operation.

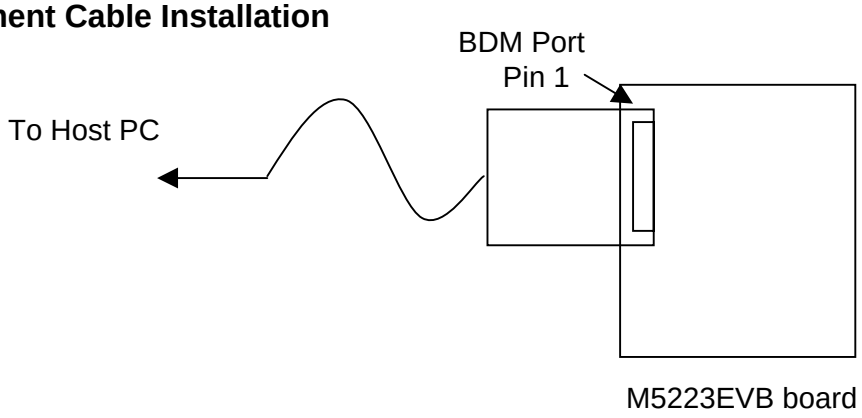
Position	MCF52235 Signal with Pull-up Applied
1	SDA
2	SCL

M52235EVB I/O Ports

BDM_PORT

The BDM PORT provides a standard ColdFire BDM / JTAG development port. The **BDM_EN** option provides for the development port mode selection between BDM or JTAG. Option **BDM_SEL** provides for a special JTAG mode port configuration that is applied to defeat the MCF52235 flash security (if enabled) for bulk erasing.

Development Cable Installation



BDM_EN Option

The BDM_EN option will select the development port mode at Reset.

Position	Development Port Mode
IN	BDM Mode (Default)
OUT	JTAG Mode

BDM_SEL Option

BDM_SEL provides BDM port signal configuration option for BDM or Special JTAG mode. Special JTAG mode is applied for tools to defeat the MCF52235 flash security.

Position	BDM Port Configuration
1-2	BDM Mode (Default)
2-3	Special JTAG

BDM Port Connector

	1	**2**	BKPT*
GND	**3**	**4**	TRST/DSCLK
GND	**5**	**6**	TCLK (From BDM_SEL option)
RSTI*	**7**	**8**	DSI
+3.3V	**9**	**10**	DSO
GND	**11**	**12**	PST3
PST2	**13**	**14**	PST1
PST0	**15**	**16**	DDATA3
DDATA2	**17**	**18**	DDATA1
DDATA0	**19**	**20**	GND
	21	**22**	
GND	**23**	**24**	CLKOUT (From BDM_SEL option)
+3.3V	**25**	**26**	

J1 Port Connector

Physical connection of the J1 Ethernet Port.

1	10/100 TX+	POE Input 3
2	10/100 TX-	
3	10/100 RX+ →	POE Input 4
4	POE Input 1	
5	POE Input 1	
6	10 /100 RX- →	
7	POE Input 2	
8	POE Input 2	

Note: POE supply will typically apply inputs 1 and 2, or 3 and 4, not both pairs. Any input may be positive or negative voltage. POE typical operating voltage is 48VDC.

MCU PORT

The MCU PORT provides user access to the MCF52235 I/O ports. Refer to the MCF52235 device reference manual for signal details. The chart indicates EVB features connected to I/O ports also. Apply associated option jumpers to isolate I/O from the EVB application if required.

	VX (VX_EN option)	**1**	**2**	IRQ1*	SW3
	GND / VSS	**3**	**4**	RSTI*	RESET SW
UART1	UTXD1	**5**	**6**	RSTO*	RESET LED
UART1	URXD1	**7**	**8**	IRQ2*	
UART1	URTS1	**9**	**10**	AN4	
UART1	UCTS1	**11**	**12**	AN5	
	PWM1	**13**	**14**	AN6	
	PWM3	**15**	**16**	AN7	
	QSPI_DOUT	**17**	**18**	AN3	
	QSPI_DIN	**19**	**20**	AN2	
	QSPI_SCK	**21**	**22**	AN1	RZ1
	QSPI_CS0	**23**	**24**	AN0	RV1
	QSPI_CS1	**25**	**26**	SDA	I2C pull
	QSPI_CS2	**27**	**28**	SCL	I2C pull
	QSPI_CS3	**29**	**30**	PWM5	
	IRQ3*	**31**	**32**	PWM7	
SW1	IRQ4*	**33**	**34**	DTIN0	LED1
	IRQ5*	**35**	**36**	DTIN1	LED2
	IRQ6*	**37**	**38**	DTIN2	LED3
ABORT SW	IRQ7*	**39**	**40**	DTIN3	LEd4
UART0	UTXD0	**41**	**42**	URTS0*	UART0
UART0	URXD0	**43**	**44**	UCTS0*	UART0
UART2	UTXD2	**45**	**46**	URTS2*	UART2
UART2	URXD2	**47**	**48**	UCTS2*	UART2
	GPT0	**49**	**50**	GPT1	
	GPT2	**51**	**52**	GPT3	
	RCON*	**53**	**54**	GND	
	VDDA	**55**	**56**	VSSA	
VRH_EN	VRH	**57**	**58**	VRL	VRL_EN
	+3.3V	**59**	**60**	+3.3V	
	IRQ8*	**61**	**62**	IRQ9*	
	IRQ10*	**63**	**64**	IRQ11*	SW2
	IRQ12*	**65**	**66**	IRQ13*	
	IRQ14*	**67**	**68**	IRQ15*	
CAN	CANTX / SYNCA	**69**	**60**	CANRX / SYNCB	CAN
	GND	**71**	**62**	GND	
PHY_LED	COL_LED	**73**	**64**	DUP_LED	PHY_LED
PHY_LED	SPD_LED	**75**	**66**	LNK_LED	PHY_LED
PHY_LED	ACT_LED	**77**	**68**	RX_LED	PHY_LED
PHY_LED	TX_LED	**79**	**80**	GND	

TROUBLESHOOTING

The M52235EVB is fully tested and operational prior to delivery. If it fails to function properly, inspect the board for obvious physical damage first.

The most common problems are improperly configured options or communications parameters.

1. Handling can damage the EVB components if ESD prevention measures are not applied. ESD damage is evident by non-operation and/or high current (>500ma) from the external power supply. The EVB power supplies will shutdown after a short while or will not be able to supply sufficient voltage with this type of damage.

2. No +3.3V indication: Verify input supply and connection to power jack or J1 for POE supply. Review PWR_SEL option setting. Verify ON-OFF switch is ON.

3. RESET indicator is ON constantly. Verify CLK_SEL option setting or clock source. Measure VDD supply for +3.3V. Verify VDD option is installed on both pins.

4. Disconnect all external connections to the board except for the wall plug and check operation again.

5. If applying a BDM or JTAG cable on the BDM Port, make sure the BDM_EN and BDM_SEL options are properly set. Verify BDM pod/cable is properly connected and aligned with Pin 1 of the BDM port. If a PC error message, review Driver installation for the cable and that correct BDM interface and device target is selected in the host software.

6. Remove BDM pod from EVB connector if the host software or connection is not operational. Otherwise, initiate host software operation of the BDM.

7. Contact support@axman.com by email for further assistance. Provide board name and describe problem.