

M52223EVB

Development Board for Freescale MCF52223 MCU

Hardware User Guide



CONTENTS

CAUTIONARY NOTES	3
TERMINOLOGY	3
FEATURES	4
REFERENCES	5
GETTING STARTED	5
DEMONSTRATION.....	5
SOFTWARE DEVELOPMENT.....	5
HARDWARE CONFIGURATION	6
POWER	6
POWER JACK.....	6
TERMINAL BLOCK.....	6
PWRSW SWITCH.....	6
VOLTAGE INDICATORS.....	7
VOLTAGE ENABLE CUT TRACES.....	7
VDD_EN OPTION HEADER.....	7
VDDA OPTION HEADER.....	7
VRH/VRL OPTION HEADER.....	7
VDDPLL OPTION HEADER.....	7
VSTDBY OPTION HEADER.....	7
VX_EN OPTION HEADER.....	8
RESET SWITCH.....	8
RESET LED.....	8
ABORT SWITCH.....	9
ABORT LED.....	9
MEMORY.....	9
SYSTEM CLOCK.....	9
RS-232 COMMUNICATIONS.....	10
UART PORTS.....	10
UART[2:0]_EN.....	10
CONNECTOR.....	11
QSPI PORT.....	11
IIC PORT.....	11
IIC PULL-UP ENABLE.....	11
USER SWITCHES.....	12
USER LED'S.....	12
LED_EN.....	12
POTENTIOMETER.....	12
LIGHT SENSOR.....	12
USB CONTROLLER	13
M52223EVB I/O PORTS	13
BDM_PORT.....	13
BDM PORT CONNECTOR.....	13
BDM_EN OPTION.....	14
JP1.....	14
MCU_PORT.....	15
TROUBLESHOOTING	16

FIGURES

Figure 1: PWR Jack.....	6
Figure 2: TB1 Terminal Block	6
Figure 3: VX_EN Option Header.....	8
Figure 4: UARTx_EN Option Header	11
Figure 5: COM Connector.....	11
Figure 6: BDM_PORT Connector	13
Figure 7: MCU_PORT Connector	15

TABLES

Table 1: Clock Select Options.....	10
Table 2: IIC Pull Enables	11
Table 3: Push Button Switches	12
Table 4: User LED's.....	12
Table 5: BDM_EN Option Header	14
Table 6: JP1 Option Header	14

REVISION

Date	Rev	Comments
October 18, 2006	A	Initial Release.
December 14, 2006	B	Corrected MCU_PORT connector pin-out and PB switch connections. Updated formatting.
August 27, 2012	C	Updated contents and formatting. Updated address

CAUTIONARY NOTES

- 1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.
- 2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.
- 3) EMC Information on the M52233DEMO board:
 - a) This product, as shipped from the factory with associated power supplies and cables, has been verified to meet with FCC requirements as a **CLASS A** product.
 - b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.
 - c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.
 - d) Attaching additional wiring to this product or modifying the product operation from the factory default as shipped may affect its performance and cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

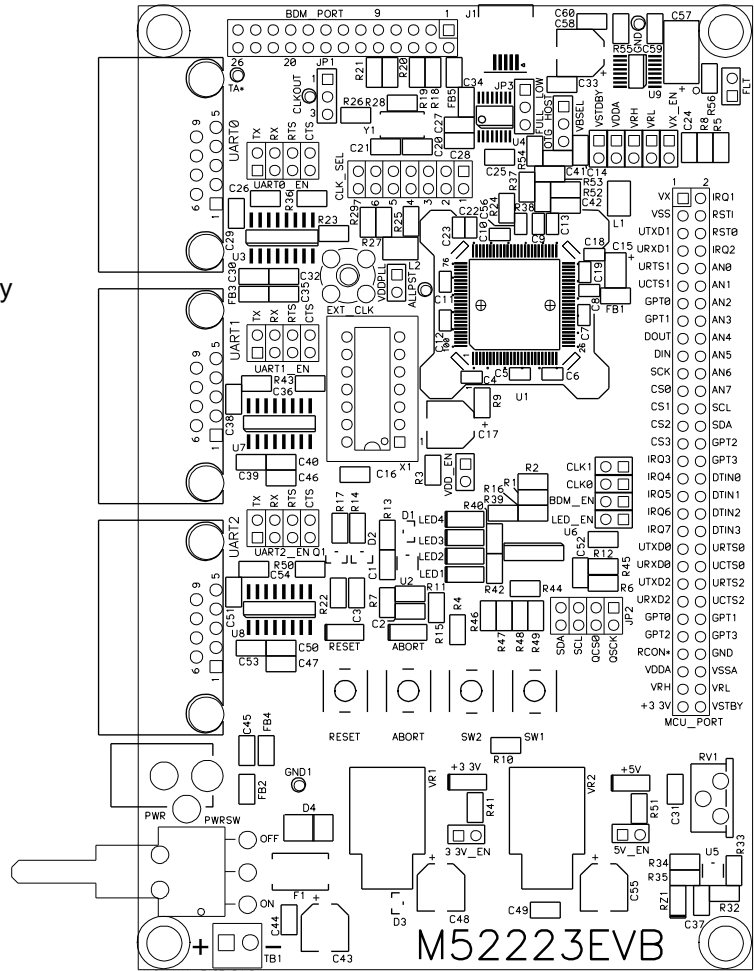
Signal names followed by an asterisk (*) denote active-low signals.

FEATURES

The M52223EVB is a low-cost development system for the Freescale MCF52223 ColdFire microcontroller. CodeWarrior Development Tools are provided to support quick and easy application development and debug. A BDM port compatible with standard ColdFire BDM / JTAG interface cables and hosting software supports applications programming and debug.

Features:

- MCF52223 CPU, 100 pins
 - 256K Byte Flash
 - 32K Byte Ram
 - 4ch, DMA Controller w/ Timers
 - 2ea. Programmable Interrupt Timer
 - 8ch, 12b ADC
 - QSPI and IIC Ports
 - USB On-The-Go (OTG) Phy
 - 3 x UART Serial Ports with DMA capability
 - 4 GPT Timers
 - BDM / JTAG Port
 - 3.3V operation
 - 80 MHz Internal Bus
- BDM / JTAG Port
- External XTAL, 48 MHz
- USB On-The-Go Bus w/ Mini AB connector
- Optional high current output on USB bus
- 3ea. RS-232 Serial Port w/ DB9-S Connector
- ON/OFF Power Switch w/ LED indicator
- RESET switch w/ indicator
- On-board Voltage Regulator, +3.3V, +5.0V
- Voltage rails enabled by cut-trace
- User Features
 - 4 User LED's w/ enable
 - 2 User Push Switches
 - 5k ohm POT
 - Light Sensor
- Connectors
 - USB Mini AB
 - 3ea. DB9 Serial Connectors
 - 2.0mm Barrel Power Input
 - 2pos, screw type, terminal block



Supplied with DB9 Serial Cable, USB cable, Support CD, and CodeWarrior Development Studio CD

Specifications:

Board Size 3.2" x 5.5"
Power Input: +7 to +15VDC, 9VDC typical

REFERENCES

The following documents should be referenced when developing with the M52223EVB. These documents are available on the MCF52223 and M52223EVB web pages (<http://www.freescale.com/coldfire>).

M52223EVB_UG.pdf	M52223EVB User Guide (this document)
M52223EVB_SCH_B.pdf	M52223EVB Schematic, Rev B
M52223EVB_Silk_B1.pdf	M52223EVB Top Silk, Rev B1
MCF52223DS.pdf	MCF52223 ColdFire Microcontroller Data Sheet
MCF52223RM.pdf	MCF52223 Integrated Microcontroller Reference Manual
CFPRM.pdf	ColdFire Programmers Reference Manual
MAX3353E.pdf	MAX3353E USB On-The-Go Charge Pump Data Sheet

GETTING STARTED

The M52223EVB single board computer is a fully assembled, fully functional development board for the Freescale MCF52223 microcontroller. The board ships with a wall plug power supply, a USB 2.0 6-in-1 cable, a P&E BDM interface cable, a 128Mb Flash Stick, and a serial cable. Provided support software for this development board is supported by the Windows 95/98/NT/2000/XP operating systems.

Development board users should be familiar with the hardware and software operation of the target MCF52223 device. Refer to the MCF52235 Integrated Microcontroller Reference Manual (MCF52223RM) for details. The purpose of the development board is to assist the user in quickly developing and debugging an application in a known working environment, to provide an evaluation platform, or as a control module for an applied system. Users should be familiar with memory mapping, memory types, and embedded software design for successful application development.

Demonstration

The M52223EVB ships from the factory with a USB demo application preloaded. Refer to the CMX-USB Device Demo for Freescale MCF5222x document on the Support CD for details on using the demo application.

Software Development

Software development is supported using a development tool connected to the BDM port. This provides real-time access to all hardware, peripherals, and memory on the board. Development tool software also provides high-level (C/C++) source code debug environment.

One method for successful application development is to load and execute the application code from RAM. The target code may then be tested and debugged using any ColdFire compatible development tool. After the application is functional and error-free in RAM, it can be ported and programmed in to Flash memory.

HARDWARE CONFIGURATION

The M52223EVB board provides a development or evaluation platform for the MCF52223 microcontroller. Following are descriptions of the components and options provided on the board.

POWER

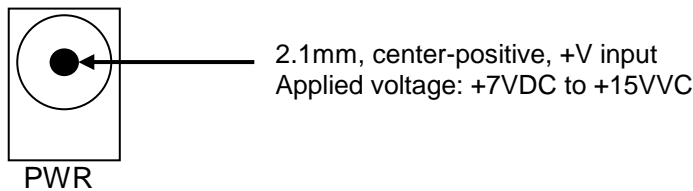
Power to the M52223EVB applies 2 on-board voltage regulators. The +3.3V regulator at VR1 supplies the MCU core voltage and supports all on-board circuitry. The +5V regulator at VR2 supplies power to the USB connector. Each regulator will supply up to 500mA of current. Both regulators are temperature and current limited to prevent damage from excessive power drain.

Input power is applied using the PWR power jack or the TB1 terminal block. The PWRSW power switch controls input voltage to the board.

Power Jack

The power jack at PWR is the default power input to the board. This connection accepts a standard 2.1mm, center-positive, barrel plug connector. +VIN should remain between +7VDC and +15VDC.

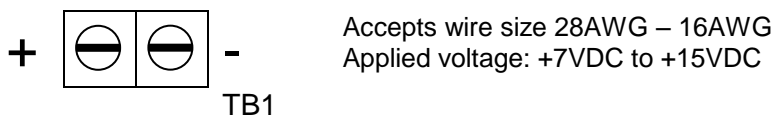
Figure 1: PWR Jack



Terminal Block

The terminal block at TB1 provides an alternate power input to the board. +VIN should remain between +7VDC and +15VDC. TB1 accepts wire sizes ranging from 28AWG to 16AWG.

Figure 2: TB1 Terminal Block



PWRSW Switch

The PWRSW connects and disconnects input voltage to the board. The silkscreen clearly marks the ON and OFF positions. This switch controls all voltage levels on the board.

Voltage Indicators

The +3.3V and +5V LED indicates availability of the associated voltage rail.

Voltage Enable Cut Traces

Power to the board is enabled by 2 cut-traces at +3.3V_EN and +5V_EN. These cut-traces are standard 2-position “Berg” headers with an embedded circuit trace providing default connection. The header is not installed in default configurations. To disconnect either voltage rail, simply cut the embedded circuit trace between the option jumper mounting holes. Install a 0.1”, 2-position option jumper and shunt to re-enable this feature.

The +3.3V rail supplies power to the MCU core and on-board circuitry. The +5V rail is used to supply power to high-power USB peripherals connected to the EVB.

VDD_EN Option Header

VDD_EN allows the user to isolate the MCF52223 device VDD pins to make measurements or to provide an alternate supply. This option is installed by default. Do not operate the EVB without the proper power supplied to the MCF52223 supply pins.

VDDA Option Header

This is a dedicated power supply input to isolate the sensitive ADC analog circuitry from the normal levels of noise present on the digital power supply. This is also the default connection for the VRH input.

VRH/VRL Option Header

These signals serve as the high (VRH) and low (VRL) reference potentials for the analog converter in the ADC. These option headers allow input of alternate ADC reference voltages.

In default configurations, VRH connects to the VDDA rail and VRL connects to GND.

VDDPLL Option Header

The VDDPLL option header provides power to the PLL and PWM module. This input is filtered to remove digital noise. Removing this shunt allows this voltage input to be isolated. In default configurations, this input connects to the +3.3V rail on the EVB.

VSTDBY Option Header

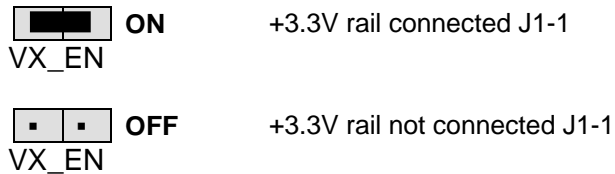
This input is used to maintain RAM contents if VDD fails below the acceptable range for device operation. The input connects to the +3.3V rail by default.

VX_EN Option Header

The VX_EN option header is a 2-pin jumper that connects the target-board, +3.3V, voltage rail to the MCU_PORT, pin 1. MCU_PORT, pin 3 is connected directly to the ground plane. This input requires a regulated +3.3V voltage source. This power input is decoupled to minimize noise input but is not regulated. Also, no protection is applied on this input and damage to the target board may result if over-driven. Do not attempt to power the target board through this connector while also applying power through the PWR connector as damage to the board may result.

Power may be sourced to off-board circuitry through the MCU_PORT. The current limitation of the on-board regulator must be considered when attempting to source power to external circuitry. Excessive current drain may damage the target board or the on-board regulator. The figure below shows the VX_EN option header connections.

Figure 3: VX_EN Option Header



CAUTION:

Do not apply power to connector J1 while also sourcing power from the PWR connector. **Otherwise, damage to the board may result.**

NOTE: Do not exceed available current supply from on-board regulator when sourcing power through connector J1 to external circuitry.

RESET Switch

The RESET switch allow the manual application of the RSTI* signal. Application of RESET halts the current operation and initializes internal registers to their default state. The previous operating state of the MCF52223 will be lost.

External reset may also be applied directly to the RSTI* signal on the MCU_PORT, pin 6.

Reset LED

RESET indicator will be ON for the duration of a valid RSTO* signal. The RSTO* signal is driven active while the MCU is in the RESET state. The RESET LED remains lit for approximately 150ms after RESET is released.

ABORT Switch

The ABORT switch allows manual application of the IRQ7 interrupt signal.

Abort LED

The ABORT LED is ON while the ABORT switch is pressed. This LED will remain ON as long as the ABORT is pressed. This LED will remain lit for approximately 450ms after the switch is released.

Memory

Memory for application development is internal to the MCF52223 MCU. This memory includes 32K bytes of SRAM and 256K bytes of Flash memory. Refer to the MCF52223RM for details on memory type and location.

System Clock

The M52223EVB target MCU accepts timing input from several sources. Input sources on this development board include: (1) an on-board, 48 MHz crystal; (2) an internal, 8MHz, RC oscillator; (3) external clock input from SMA connector or 14DIP socket. The SMA connector and DIP socket are not installed in default configurations.

The internal Phase-Locked Loop (PLL), Multiplication Factor Divider (MFD), and Reduction Factor Divider (RFD) may be used to synthesize frequencies ranging from 1X to 18X the input frequency, up to the 80MHz maximum internal system frequency.

PLL settings are under user application control and may be changed while the application is running. However, changing the target MCU clock frequency or COM baud rate while the application executes may cause loss of communications.

CAUTION:

Communications with the target may be lost if the application changes clock frequency or baud rate during execution

Option jumpers set timing selection and configuration as outlined in Table 1 below. Refer to the MCF52223RM for details on timing input and setup.

Table 1: Clock Select Options

Clock Type		Clock Mode		CLKSEL Option Setting					
Source	PLL	CLK0	CLK1	1	2	3	4	5	6
Y1 (48Mhz)	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Y1 (48Mhz)	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
INT OSC	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
INT OSC	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF
EXT CLK	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON
EXT CLK	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON
X1	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF
X1	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF

Notes: Y1 refers to the external crystal
 INT OSC refers to the MCF52223 internal 8 MHz relaxation oscillator.
 EXT CLK refers to the unpopulated SMA connector.
 X1 refers to the clock oscillator socket. Supports 3.3V full and half size clocks.
 CLKSEL option header positions 4 – 6 are not populated in default configuration.

RS-232 Communications

The M52223EV board provides 3 UART ports, 1 QSPI port, 1 IIC port, and 1 USB OTG port. RS-232 communication is supported through UART[2:0] connectors and through the MCU_PORT connector. QSPI and IIC communications are supported solely through the MCU_PORT connector. The UARTx_EN option header enables SCI functionality between the MCU and the associated UARTx connector.

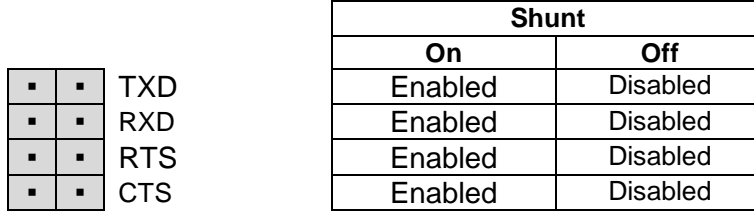
UART Ports

An RS-232 transceiver provides RS-232 to TTL/CMOS logic level translation between the UARTx connector and the MCU. The UARTx connector is a 9-pin Dsub, right-angle connector. A ferrite bead on shield ground provides conducted immunity protection. Communication signals TXDx, RXDx, CTSx, and RTSx are routed from the transceiver to the MCU. These signals are also available at the MCU_PORT connector. RTS is biased for correct 2-wire operation.

UART[2:0]_EN

The UARTx_EN option header individually connects and disconnects UARTx signals between the MCU and the SCI transceiver. Each communications channel, UART[2:0] applies an individual UARTx_EN option header. Figure 4 below shows various options for each setting.

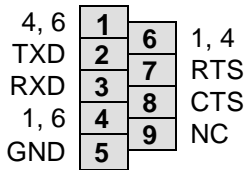
Figure 4: UARTx_EN Option Header



Connector

A standard 9-pin Dsub connector provides external connections for each UARTx port. The Dsub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. The DB9 connector pin-out is shown below.

Figure 5: COM Connector



Female DB9 connector that interfaces to the ColdFire internal SCI1 serial port via the RS232 transceiver.

Pins 1, 4, and 6 are connected together.

QSPI Port

QSPI signaling connects directly between the MCU and the MCU_PORT connector. Refer to the MCF52223RM for details on using the QSPI interface.

IIC Port

IIC signaling connects directly between the MCU and the MCU_PORT connector. Refer to the MCF52223RM for details on using the IIC interface.

IIC Pull-up Enable

The JP2 option header allows the user to apply pull-ups on IIC signals. This option block applies 4.7k ohm pull-ups to +3.3V for the MCF52223 I2C serial port signals, SDA and SCL. These signals must be enabled for proper IIC serial bus operation.

Table 2: IIC Pull Enables

Position	MCF52223 Signal
1	QSPI_SCK/SCL
2	QSPI_CS0/SDA
3	SCL
4	SDA

User Switches

Two, active-low, push-button switches (SW1, SW2) support user input. Pull-ups applied to both SW's prevent spurious operation. SW1 connects to the IRQ5 input on the MCU; SW2 connects to IRQ1 as shown in Table 3 below.

Table 3: Push Button Switches

Switch	Signal
SW1	IRQ5*\USB_VBUSVLD
SW2	IRQ1*\SYNCA\USB_ALT_CLK

User LED's

The M52223EVB applies four user LED's as output indicators. These LED's connect to the MCF52223 DTIN[3:0] signals as detailed in Table 4 below. These signal pins may be configured for GPIO or Timer functionality to drive the LEDs. Each LED is buffered to prevent loading MCF52223 I/O port pins. The LED_EN option header enables the LED buffer.

Table 4: User LED's

	COLOR	OPERATION	DEFAULT CONDITION
LED1	Green	DTIN0 status, high = ON	ON
LED2	Green	DTIN1 status, high = ON	ON
LED3	Green	DTIN2 status, high = ON	ON
LED4	Green	DTIN3 status, high = ON	ON

LED_EN

Install the LED_EN option jumper to enable user LED indicators LED[4:1]. Remove this option jumper to disable LED[4:1] operation.

Potentiometer

A 5k ohm, single-turn, thumb-wheel type, potentiometer at RV1 provides continuous, variable resistance input for user applications. The potentiometer connects between +3.3V and GND with the center tap providing the divider output. This center tap connects to MCU input, AN0.

Light Sensor

A surface-mount phototransistor, at RZ1, provides light sensitive, variable input for user applications. Current flow within the phototransistor is inversely proportional to light intensity incident on the surface of the device. A rail-to-rail OP amp at U5 boosts the photocell output to useable levels. This signal is available to the MCU on signal AN1.

USB CONTROLLER

The M52223EVB supports the USB 2.0, On-The-Go (OTG) protocol. A Mini AB connector supports connection of USB peripherals to the EVB. The cable type connected to the board determines host or peripheral mode. A configurable charge-pump at U4 applies the pull-up/pull-down resistor configuration. This charge pump also provides the OTG VBUS current when in HOST mode. Pull-up and pull-down configuration may also be applied to the USB data lines independently of the charge-pump.

The VBUS_SEL option header allows the user to configure the voltage source used to power VBUS when in HOST mode. Setting the VBUS_SEL jumper to the HOST position sources VBUS from the on-board voltage regulator at VR2. The on-board regulator will supply up to 500mA of current on VBUS when selected. The OTG position selects VBUS from the charge-pump at U4. The charge-pump sources a minimum of 8mA on VBUS when selected.

The MCU includes an OTG compliant physical layer interface (PHY). The device also provides the necessary signals to connect to an external USB PHY. These USB signals are available at the MCU_PORT connector. Refer to the MCF52223RM for complete details on the USB OTG operation.

Refer to the MAX3353E data sheet for details on the operation of the configurable charge-pump.

M52223EVB I/O PORTS

BDM_PORT

The BDM_PORT provides a standard ColdFire BDM / JTAG development port. The BDM_EN option header allows the user to select between BDM and JTAG development cable mode. The JP1 option header provides for a special JTAG-mode port configuration that is used to defeat the MCF52223 flash security (if enabled) for bulk erasing.

BDM Port Connector

Figure 6: BDM_PORT Connector

NC	1	2	BKPT*
GND	3	4	DSCLK
GND	5	6	TCLK (JTAG)
RSTI*	7	8	DSI
+3.3V	9	10	DSO
GND	11	12	PST3
PST2	13	14	PST1
PST0	15	16	DDATA3
DDATA2	17	18	DDATA1
DDATA0	19	20	GND
NC	21	22	NC
GND	23	24	CLKOUT (BDM)
+3.3V	25	26	TA*

BDM_EN Option

The BDM_EN option will select the development port mode at RESET.

Table 5: BDM_EN Option Header

Position	Development Port Mode
ON	BDM Mode (Default)
OFF	JTAG Mode

JP1

BDM_SEL provides BDM port signal configuration option for BDM or Special JTAG mode. Use the Special JTAG mode to defeat the MCF52223 flash security.

Table 6: JP1 Option Header

JP1		BDM Mode (Default)
JP1		Special JTAG

MCU_PORT

The MCU PORT provides user access to the MCF52223 I/O ports. Refer to the MCF52223 Integrated Device Reference Manual for signal details.

Figure 7: MCU_PORT Connector

VX	1	2	IRQ4*/USB_PULLUP/GPIO
GND	3	4	RSTI*
UTXD1/USB_SPEED/GPIO	5	6	RSTO*
URXD1/USB_OE*/GPIO	7	8	IRQ2*/USB_SESSVLD/GPIO
URTS1*/SYNCB/UTXD2/GPIO	9	10	AN0/GPIO
UCTS1*/SYNCA/URXD2/GPIO	11	12	AN1/GPIO
(also pin 49) GPT0/PWM1/GPIO	13	14	AN2/GPIO
(also pin 50) GPT1/PWM3/GPIO	15	16	AN3/GPIO
QSPI_DOUT/UTXD1/GPIO	17	18	AN4/GPIO
QSPI_DIN/URXD1/GPIO	19	20	AN5/GPIO
QSPI_SCK/SCL/URTS1*/GPIO	21	22	AN6/GPIO
QSPI_CS0/SDA/UCTS1*/GPIO	23	24	AN7/GPIO
QSPI_CS1/USB_PULLUP/GPIO	25	26	SCL/USB_DMI/UTXD2/GPIO
QSPI_CS2/USB_DM_PDOWN/GPIO	27	28	SDA/USB_DPI/URXD2/GPIO
QSPI_CS3/SYNCA/USB_DP_PDOWN/GPIO	29	30	GPT2/PWM5/GPIO (also pin 51)
IRQ1*/SYNCA/USB_ALT_CLK/GPIO	31	32	GPT3/PWM7/GPIO (also pin 52)
IRQ3*/USB_SESEND/GPIO	33	34	DTIN0/DTOUT0/PWM0/GPIO
IRQ5*/USB_VBUSVLD/GPIO	35	36	DTIN1/DTOUT1/PWM2/GPIO
IRQ6*/USB_ID/GPIO	37	38	DTIN2/DTOUT2/PWM4/GPIO
IRQ7*/GPIO	39	40	DTIN3/DTOUT3/PWM6/GPIO
UTXD0/USB_SUSPEND/GPIO	41	42	URTS0*/USB_VBUSD/GPIO
URXD0/USB_RCV/GPIO	43	44	UCTS0*/USB_VBUSE/GPIO
UTXD2/USB_SE0/GPIO	45	46	URTS2*/USB_VBUSDIS/GPIO
URXD2/USB_DATA/GPIO	47	48	UCTS2*/USB_VBUSCHG/GPIO
GPT0/PWM1/GPIO	49	50	GPT1/PWM3/GPIO
GPT2/PWM5/GPIO	51	52	GPT3/PWM7/GPIO
RCON*	53	54	GND
VDDA	55	56	VSSA
VRH	57	58	VRL
3.3V	59	60	VSTBY

NOTE: MCU_PORT silkscreen applies only primary signal name as indicated in bold above.

TROUBLESHOOTING

The M52223EVB is fully tested and operational before shipping. If it fails to function properly, inspect the board for obvious physical damage first. Verify the communications setup as described under GETTING STARTED.

1. Most common problems are related to improperly configured options or communications parameters.
2. Verify default option settings and RESET the board.
3. Make sure the RSTI* line is not being held low and that RESET indicator is not ON.
4. Verify the PC COM port is working by substituting a known good serial device or by doing a loop back diagnostic.
5. Verify the +3.3V and +5V voltage indicators are ON.
6. Verify input power is connected. Using a multi-meter, measure at least +7V across component D4.
7. If voltage indicators are not lit, or if no voltage is measured across component D4, verify the wall plug connections to AC outlet and the PWR jack power connector.
8. Disconnect all external connections to the board except for UART0 to the PC and the wall plug and check operation again.
9. If applying a BDM or JTAG cable on the BDM Port, make sure the BDM_EN option is properly set.
10. Ensure that the BKPT* line is not being asserted by an active BDM interface cable applied to the BDM connector.

Contact support@axman.com by email for further assistance. Provide board name and describe problem.