EVB9S12NE64

Development Board for the Freescale M9S12NE64

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Cautionary Notes

1) Electrostatic Discharge (ESD) prevention measures should be applied whenever handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing reserves the right to make changes without further notice to any products to improve reliability, function or design. Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the EVB9S12NE64 board:

a) This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of CE and the FCC as a **CLASS A** product.

b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

c) In a domestic environment this product may cause radio interference in which case the user may be required to take adequate prevention measures.

d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

Terminology

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

> Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.
>
> Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be idled by installing on 1 pin so they will not be lost.

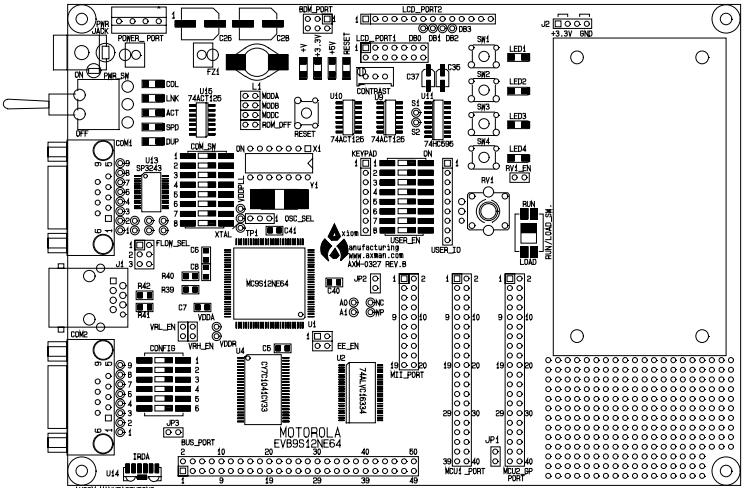
This development board applies hardwired option selections (VRL_EN and CUTAWAY 1 – 3). These option selections apply a circuit trace between the option pads to complete a default connection. This type connection places an equivalent Jumper Installed type option. The circuit trace between the option pads maybe cut with a razor blade or similar type knife to isolate the default connection provided. Applying the default connection again can be performed by installing the option post pins and shunt jumper, or by applying a wire between the option pads.

FEATURES

The EVB9S12NE64 is an evaluation or development board for the Freescale M9S12NE64 microcontroller. Development of applications is quick and easy with the included DB9 serial cable, sample software tools, examples, and debug monitor. The prototyping area provides space to apply the CPU I/O to your needs. The BDM port is provided for development tool application and is compatible with HCS12 BDM interface cables and software.

Features:

- MC9S12NE64 CPU
  - * 64K Byte Flash
  - * 8K Bytes Ram
  - * 70 I/O lines (112 pins)
  - * 10/100 EMAC and EPHY
  - * 4 channel Timer w/PWM
  - * 8 Channel 10 BIT A/D
  - * SPI and I2C Serial Ports
  - * 2 x SCI Serial Ports
  - * 21 Key Wake-up Ports
  - * BDM Port
  - * Clock generator w/ PLL
  - * 0 - 25Mhz operation
- 25MHz reference Crystal oscillator
- External Clock oscillator optional
- Regulated +3.3V and 5V power supplies
- COM1 Serial Port w/ RS232 DB9-S Connector
  - * SCI0 Serial Port
- COM2 Serial Port w/ RS232 DB9-S Connector
  - * SCI1 Serial Port
- IRDA wireless port on SCI1
- 10/100T Ethernet Port, 802.3
- ON/OFF switch w/ Power Indicators
- Option Switches for I/O assignments
- User Components Provided
  - * 4 LED Indicators (PTF0-3)
  - * 4 Push Switches (PTA4-7)
  - * LCD PORT (SPI)
  - * Keypad Port
- MCU PORT1 and 2 connectors provides all CPU digital I/O
- BUS PORT connector provides address/data and control in Expanded modes
- Breadboard and Prototype Areas
- Supplied with DB9 Serial Cable, Ethernet cable, Utility and Support CD, Manuals, and Wall plug type power supply.



EVB9S12NE64

Specifications:
Board Size 5.0 x 7.0 inches
Power Input: +6 - +16VDC, 9VDC typical
Current Consumption: 120ma @ 9VDC input typical

The EVB9S12NE64 is provided operating the Freescale binary serial monitor. The monitor allows serial interface to host based development environments for source level debugging operations.

GETTING STARTED

The EVB9S12NE64 single board computer is a fully assembled, fully functional development board for the Freescale MC9S12NE64 microcontroller. Support software for this development board is provided for Windows 95/98/NT/2000/XP operating systems.

Development board users should also be familiar with the hardware and software operation of the target HCS12 device, refer to the provided Freescale User Guide for the device and the HCS12 Reference Manual for details. The development board purpose is to assist the user in quickly developing an application with a known working environment or to provide an evaluation platform for the target HCS12. Users should be familiar with memory mapping, memory types, and embedded software design for the quickest successful application development.

Application development maybe performed by applying the embedded serial interface monitor, or by applying a compatible HCS12 BDM cable with supporting host software. The monitor provides an effective and low cost debug method.

Special Operating Notes

The EVB9S12NE64 board provides Expanded Wide Mode operation of external on-board SRAM development memory. For compatibility with the Ethernet 100T operation of the NE64 device, the expanded bus will operate at 25Mhz in a lab environment (25 degrees C). This bus operating frequency is well beyond the specified expanded bus operating frequency of 16Mhz and should not be applied in user designs.

The Expanded Wide Mode operation on the EVB board requires the MODE register EMK bit to be enabled for proper operation of the external SRAM board memory.

Reference Documentation

Reference documents are provided on the support CD in Acrobat Reader format.

M9S12NE64 user manual
CPU12 core user manual with instruction set
EVB9S12NE64_SCH_B.pdf – EVB9S12NE64 board schematics
AN2548 Serial Monitor application note

EVB9S12NE64 Startup

Follow these steps to connect and power on the board for the default Monitor operation.

1) With EVB board ON/OFF switch in the off position, configure these options for default settings:

   MODA, MODB, MODC, and ROM_OFF option jumpers Open or Idle.

   RUN/LOAD Switch in the LOAD position.

FLOW_SEL option jumpers in default positions (no flow enabled).

COM_Switch positions 1 and 2 ON, other as needed for application.

CONFIG_Switch as needed for application.

USER_Enables as needed for application.

2) Connect the EVB COM1 port to the host PC with the 9 pin serial cable.

3) Connect the EVB POWER JACK with the provided power supply and install the power supply into a local wall or power strip outlet.

4) Turn the EVB board ON/OFF switch to the ON position and observe the +V, +3.3V, and +5V indicators are ON.

5) Launch the desired monitor IDE software on the host PC and establish communication with the EVB target. Verify target is the Serial Monitor in the IDE software if optional.

You are now ready to load and debug your application code or examples.

MONITOR OPERATION

Refer to application note AN2548 for complete details of the Serial Monitor. The monitor firmware resides in the 9S12NE64 flash memory from addresses 0xF800 > 0xFFFF (2K bytes). Monitor operation applies the SCI0 serial port and internal ram space starting at 0x3FFF (grows downward) for Stack and variables. All other memory space and peripherals are available to the user.

MONITOR MEMORY MAP

Address (Hex)	Memory Type
0000 > 03FF	NE64 Registers
0400 > 1FFF	External SRAM if enabled
2000 > 3FFF	Internal SRAM, STACK = 3FFF
4000 > F77F	User Internal flash Memory (Program space)
F780 > F7FF	User Interrupt vectors
F800 > FFFF	Monitor firmware (protected)

RUN / LOAD Switch

The RUN/ LOAD switch allows selection of monitor operation or user code application during RESET condition. If the User Reset vector at address 0xFBFE/F is programmed to a non-erased state value and the RUN/LOAD switch is in the RUN condition, the monitor will apply the user Reset vector to start the user application. The RUN/LOAD switch allows the user to force the monitor to start when the LOAD position is selected.

EVB9S12NE64 OPERATION

The EVB9S12NE64 board provides many input and output features to assist in application development. These features may be isolated from the applied HCS12 I/O ports by the option switches or jumpers. This allows alternate use of the HCS12 I/O ports for other application and connection on the MCU1_PORT or MCU2_GP_PORT connectors. Caution should be observed so that the HCS12 I/O port pin applied to an on board feature is not also applied to external components by the user.

MODE OPTIONS

The EVB board provides options for Mode selection or memory configuration during power-on or Reset. User should properly apply these options for correct development mode and memory map.

MODA, MODB, MODC

The MODA, MODB, and MODC options provide selection of the default operating mode of the 9S12NE64 at Reset. Default option position for the MODA, MODB, and MODC options is open or idle. The default setting places the NE64 in normal Single-chip Mode for operation of the serial monitor located in the internal flash memory. Some configuration settings provided by the Mode selection can be modified in software during initialization, refer to the 9S12NE64 user documents for more details. See the MODE CHART below for valid Mode option settings on the EVB9S12NE64 board.

ROM_OFF

The ROM_OFF option is default open or idle. Installation of the ROM_OFF option will disable the internal flash memory of the NE64 device at Reset. This option should only be installed during application of Background Debug Module (BDM) type tools.

MODE_CHART

MODE Option	Option Position	Operating Notes
MODA / MODB	Open (Default)	Single-chip Mode (Expanded Modes maybe configured in software during initialization).
MODC	Open (Default)	Special Modes enable. Install with BDM cable application only.
ROM_OFF	Open (Default)	Internal Flash Memory Disable. Install with BDM application only.

POWER SUPPLY

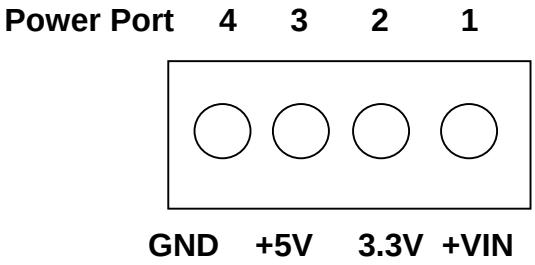
Input power is applied by external connection to the Power Jack or Power Port terminal block. The input supply is enabled to the voltage regulator by the ON_OFF switch. The regulators are protected from reverse voltage by diode D2 and current limited by fuse FZ1. Input voltage is regulated to +3.3V supply by VR1. With +5 to +16VDC applied and the ON_OFF switch in the ON position, the +V, +3.3V, and +5V Indicators should be ON.

FUSE – FZ1

Fuse FZ1 will open during an over current condition. The cause of an over current condition that opens FZ1 should be corrected before fuse replacement. FZ1 is a 5x20mm 500ma slow blow type fuse.

Power Port

Power Port terminal block provides access to the +VIN, +5V, +3.3V, and GND (power ground) supplies. The +VIN connection is not switched by the ON-OFF switch or fused and is directly connected to the Power Jack. The +3.3V position can source 200ma to external circuits. Applying +3.3V or +5V externally to power the board from the Power Port should not be performed. If the user needs more power, an additional voltage regulator or source should be applied with a common ground connected at the Power Port GND connection.



Power Jack

The Power Jack provides the default power input to the board. The jack accepts a standard 2.0 ~ 2.1mm center barrel plug connector (positive voltage center) to provide the +VIN supply of +5 to +25 VDC (+9VDC typical).

+Volts, 2mm center

PWR_SW – ON/OFF

The PWR Switch provides board power ON and OFF control. The +VIN supply from either the PWR Switch or the POWER_PORT is applied via the switch.

VRH_EN and VRL_EN

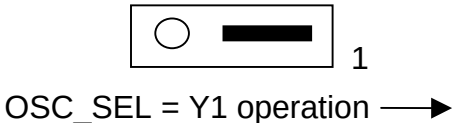
VRH and VRL analog signals are connected to VDDA and Ground potentials respectfully by the VRH_EN and VRL_EN option positions. The VRL_EN signal has a wired connection that may be isolated from the default potentials by a cut with a razor blade or knife between the option pads on the development board. Alternate VRH or VRL signals may then be applied at the ANALOG Port. To restore the default connection, a 1x2 pin post header can be installed to allow option jumper use or a wire jumper can be installed between the option pads.

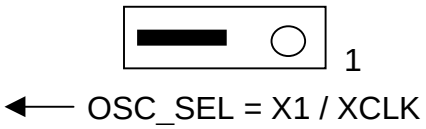
RESET Operation

The RESET switch, BDM if applied, or NE64 device generate the HCS12 RESET* signal. The RESET indicator will light for the duration of the active RESET signal. Mode configuration options are input by the NE64 during the reset.

OSC_SEL

The OSC_SEL option jumper provides selection between the Y1 crystal oscillator circuit and an external X1 clock source or MCU2_GP_Port XCLK signal. The Y1 25Mhz crystal oscillator is selected by default.





X1 CLOCK OSCILLATOR

The X1 socket is provided to install a standard 3.3V compatible CAN type clock oscillators so that alternate reference frequencies maybe applied to the NE64. User should refer to the NE64 device user manual for information on frequency selection.

X1 clock signal XCLK is provided at the MCU2_GP_Port pin 24. The port pin may be applied to output the X1 clock or to input a 3.3V peak to peak clock signal. If a signal is input to the XCLK connection on the MCU2 port, the X1 clock oscillator should not be installed in the socket. Note that the X1 clock XCLK signal maybe applied for output to the MCU2_GP_Port without application to the NE64 by placing the OSC_SEL option in the Y1 position.

EXTERNAL BUS

The EVB board provides an external address and data bus with control signals. Bus operation requires the NE64 MODE register EMK bit to be set. EVB board Bus application is dedicated to the 512K Byte external ram memory access to provide development memory. EVB board operation allows 25Mhz external bus operation at 0 clock stretch cycles for development purposes. User should note that the NE64 device has a 16Mhz rated external bus capability and that 25Mhz operation should not be expected in NE64 product designs. Refer to the EVB board schematic drawing for bus connection details.

CONFIG Switch

The CONFIG switch provides options for the EVB9S12NE64 development board external bus, external SRAM, LCD Ports, Ethernet PHY status indications, and IRDA shut down features.

CONFIG_SW	OPERATION	Operation Notes
1	Expanded Bus Logic Enable	ON = Expanded Wide BUS is enabled and BUS_PORT is active. NE64 Ports A, B, E, and K applied for BUS operation. NE64 should be in Expanded Wide Mode with MODE EMK bit enabled for operation. OFF = Bus logic is disabled and external memory will not operate.
2	RAM Select 1 = All expanded memory space	ON (2 ON, 3 and 4 OFF) = External ram is available for the entire accessible external expanded memory space.
3	RAM Select = XCS*	ON (3 ON, 2 and 4 OFF) = External ram is available for the XCS* chip select memory space. NE64 MODE must be Expanded Wide with EMK bit set.
4	Ram Select = ECS*	ON (4 ON, 2 and 3 OFF) = External ram is available for the NE64 Flash space (MISC = flash off, EMK = ON) Note: Only applied with BDM.
5	LCD Port Enable	ON = LCD Ports are enabled on the NE64 SPI port. Port S7 / SS* signal operation will access the LCD port shift register. OFF= SPI is not applied to the LCD Ports.
6	Ethernet Status Enable	ON = Ethernet PHY status indicators TX_RX, LNK, 100, DUP, and COL are enabled on NE64 Port L 0 – 4. NE64 PHY register settings must also enable operation. Note that the status indicators may also be applied under Port L manual operation if wanted. OFF = Ethernet status indicators are not enabled on NE64 Port L.

J1 Ethernet Port

J1 provides the standard RJ45 endpoint connection for a 10/100T type Ethernet port. The Ethernet cable provided with the EVB board is a CAT5E crossover type for connection directly to a PC type Ethernet port. A standard CAT5E Ethernet cable should be applied to connect a HUB type Ethernet port. The port is driven directly from the NE64 EPHY connections. Refer to board schematic for connection details and the MC9S12NE64 EPHY manual for additional details.

STATUS Indicators

The EVB board provides 5 Ethernet status indicators, TX_RX, LNK, 100, DUP, and COL, that are controlled by NE64 port PTL0 – 4 outputs respectfully. CONFIG switch position 6 must be ON to enable these indicators on the EVB board. Ethernet status indicator operation is provided by NE64 PHY control or the user may apply under application software control of the individual PTL ports. Active port level is logic 0 or 0V.

Indicator	Color	Control Port	Operation Indication
ACT	RED	PTL0	Transmit or Receive in progress
LNK	GREEN	PTL1	Network Link is detected
SPD	GREEN	PTL2	100 base Network detected.
DUP	GREEN	PTL3	Full duplex Network detected
COL	RED	PTL4	Network experiencing collisions, trouble detected

COM Ports

The EVB9S12NE64 provides two RS232 type COM1 / 2 ports or a RS232 COM1 port and an IRDA type communication port. COM1 or COM2 may be optioned with flow controls with the FLOW_SEL options. COM_SW options enable the communication and flow control connections in hardware. User must apply correct software operation to the associated SCI port for the communication type selected.

COM_Switch

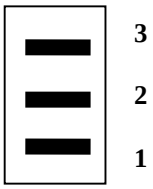
The COM_SW provides NE64 I/O port to communication peripheral connections on the evaluation board. This allows the user to apply the provided communication transceivers and ports, or to apply the associated I/O to other purposes. The switch positions and FLOW_SEL options should be reviewed first if any operational problems are encountered with the COM1, COM2, or IRDA ports.

COM_SW	HCS12 Port	COM Signal	EVB I/O Port Connection	Operation Notes
1	PTS01/RXD0	COM1 RXD IN	MCU2_GP pin 22	SCI0 to COM1 RS232 RCV
2	PTS1/TXD0	COM1 TXD OUT	MCU2_GP pin 21	SCI0 to COM1 RS232 XMT
3	PTS2/RXD1	COM2 RXD IN	MCU2_GP pin 30	SCI1 to COM2 RS232 RCV Note: Switch position 7 must be open
4	PTS3/TXD1	COM2 TXD OUT	MCU2_GP pin 29	SCI1 to COM2 RS232 XMT Note: Switch position 8 must be open
5	PTL5	COM1 RTS OUT	MCU1 Pin 30	NE64 Port L5 output is RTS signal output. See FLOW_SEL options
6	PTG7	COM1 CTS IN	MCU2_GP pin 2	NE64 Port G7 input is CTS signal input. See FLOW_SEL options
7	PTS2/RXD1	IRDA RXD IN	MCU2_GP pin 30	SCI1 to IRDA RCV Note: Switch position 3 must be open
8	PTS3/TXD1	IRDA TXD OUT	MCU2_GP pin 29	SCI1 to IRDA XMT Note: Switch position 4 must be open

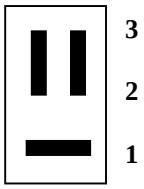
FLOW_SEL Options

The FLOW_SEL option provides configuration of the RTS / CTS flow control signals to the COM1 and COM2 port. FLOW Selection requires NE64 Port L5 to be enabled by the COM Switch position 5 as the RTS output and NE64 Port G7 to be enabled by the COM Switch position 6 as the NE64 board CTS input. User application software must also support the flow control operation of RTS / CTS signaling on PTL5 and PTG7. Following are the 3 basic option settings:

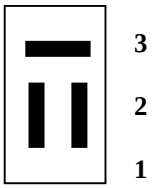
FLOW_SEL Idle, no RTS / CTS



FLOW_SEL with COM1 RTS / CTS enabled



FLOW_SEL with COM2 RTS / CTS enabled



RTS signal active output level is logic 0. User should place port PTL5 at logic low (0) to enable the RTS signal and reception of bytes if applied. User should apply a logic high signal under software control inform host or connected RS232 device to STOP transmitting (stop sending incoming bytes).

CTS signal active input level is logic 0. User should apply software to detect a logic high signal on Port PTG7 and STOP transmitting bytes to the host or connected device to implement hardware flow control. Detection of a logic low input indicates the host is ready to receive bytes and the user (NE64) may transmit.

COM1

The COM1 port provides standard 9 pin connection with RS232 type interface to the HCS12 SCI0 peripheral. Refer to the COM_SW for enabling the HCS12 RXD0 and TXD0 signals applied to this port. Refer to the COM_SW and FLOW_SEL options for enabling RTS/CTS flow controls on this port. The COM1 port is applied by default with the embedded Monitor. HCS12 SCI0 TXD0 and RXD0 signals are converted to RS232 levels by U13 and provided to the COM1 connector. The HCS12 PTL5 and PTG7 signals may be applied for the optional RTS/CTS flow control on this port. Following is the DB9S connection reference.

COM1

1	**1**		X
TXD0	**2**	**6**	6
RXD0	**3**	**7**	CTS IN
4	**4**	**8**	RTS OUT
GND	**5**	**9**	9

The **COM-1** port is a Female (socket type) DB9 connector.

Pins 1, 4, and 6 connected for status null to host.

Pins 7 and 8 optioned by COM_SW and FLOW_SEL

COM SW positions 1 and 2 will isolate the HCS12 SCI0 signals from the transceiver.

The 1, 4, 6, and 9 pins provide RS232 status. The status pins 1, 4, and 6 are connected on the on the bottom of the development board to provide a NULL status returned to the host.

DB9 connector pin locations are provided access pads behind the connector on the EVB board. User may isolate the connection pads by cutting the associated circuit trace on the bottom of the board. The user may then apply status connections to the host by applying HCS12 I/O signals and additional **RS232 level conversion.**

COM2

The COM2 port provides standard 9 pin connection with RS232 type interface to the HCS12 SCI1 peripheral. Note that the HCS12 SCI1 signals are shared with COM2 and the IRDA port. Refer to the COM_SW for enabling the HCS12 RXD1 and TXD1 signals applied to this port. Refer to the COM_SW and FLOW_SEL options for enabling RTS/CTS flow controls on this port. HCS12 SCI1 TXD1 and RXD1 signals are converted to RS232 levels by U13 and provided to the COM2 connector. The HCS12 PTL5 and PTG7 signals may be applied for the optional RTS/CTS flow control on this port. Refer to the COM_SW and FLOW_SEL options for proper option selections for this port. Following is the DB9S connection reference.

COM2

1	**1**		X	The **COM-2** port has a Female (socket type) DB9 connector.
TXD1	**2**	**6**	6	
RXD1	**3**	**7**	CTS IN	**Pins 1, 4, 6 connected for status NULL to host.**
4	**4**	**8**	RTS OUT	
GND	**5**	**9**	9	**Pins 7 and 8 optioned by COM_SW and FLOW_SEL**

COM SW positions 3 and 4 will isolate the HCS12 SCI1 signals from the COM2 port transceiver.

The 1, 4, 6, 7, 8, and 9 pins provide RS232 flow control and status. These pins are connected on the on the bottom of the development board to provide a NULL status and flow control returned to the host.

DB9 connector pin locations are provided access pads behind the connector on the EVB board. User may isolate the connection pads by cutting the associated circuit trace on the bottom of the board. The user may then apply status connections to the host by applying HCS12 I/O signals and additional **RS232 level conversion.**

IRDA Port and JP3

The IRDA port provides the HCS12 SCI1 operation of a 115.2K baud compatible IRDA interface. An IRDA transceiver is applied to provide up to 30 inches of wireless IRDA link (line of sight, indoors only). The HCS12 SCI1 module must be configured for IRDA communication to apply this port. See the COM_SW option positions 3, 4, 7, and 8 for properly enabling the IRDA port hardware with the SCI1 module.

The IRDA port has an optional Shut Down control option that may be enabled by installing the JP3 option jumper. HCS12 port L6 will provide the shutdown control signal when JP3 is installed. User application software must provide the shutdown control operation with JP3 installed. IRDA shut down is accomplished by a logic 1 (+3.3V) signal being applied. IRDA is enabled by default.

LCD PORT1 and 2

The LCD_PORT(S) interface are connected to the HCS12 SPI-0 port and are enabled by CONFIG Switch position 5 ON. The interface applies a 5Volt level serial shift register to convert the data to parallel interface for LCD input. This is required due to the fast timing characteristics of the HCS12 data bus and the slow timing of the standard LCD Modules. Example LCD Port assembly language driver software is provided on the support CD to demonstrate typical LCD module operation using this technique.

The interface supports all OPTREX™ DMC series and similar displays with up to 80 characters in 4 bit bus mode and provides the most common pin configuration for a dual row rear mounted display connector (LCD_PORT1) or an in-line connector type (LCD_PORT2). Only one connector maybe applied at a time for LCD connection. The LCD Module is configured in a Write only mode, it is not possible to read current cursor position or the busy status back from the module.

The LCD module VEE or contrast potential is adjustable by the CONTRAST potentiometer between –5V and +5V. The Axiom Mfg. HC-LCD module is compatible for connection to LCD_PORT1.

LCD_PORT1 Connector

+5V	2	1	GND
RS	4	3	VEE-Contrast
EN	6	5	R/W-GND
DB1	8	7	DB0
DB3	10	9	DB2
DB5	12	11	DB4
DB7	14	13	DB6

SPI data bit definitions to LCD Port:
D0 - D3 = DB4 - 7, LCD data in 4 bit mode.
D4 - D5 = Spare pins S1 and S2, not connected
D6 = RS, 0 = LCD Command, 1 = LCD Data
D7 = EN, 1 = LCD enable.
DB0 -DB3 are not applied and have 10K pull-down resistance.

LCD_PORT2 Connector has the same pin number and signal association in a single row connector.

The LCD write requires 3 SPI transfers. Transfer 1 provides data 0 - 3 and RS (register select) value. Transfer 2 provides the same data with the EN (D7) bit set. Transfer 3 provides same data with the EN bit clear.

I2C EEPROM Memory

A 2432 type I2C compatible EEprom is provided on the EVB board for user application. The EEprom is made available to the 9S12NE64 ports PJ6/SDA and PJ7/SCL pins by the EE_EN option jumper. Install both option jumpers for EEprom access.

KEYPAD

The KEYPAD connector provides interface for applying a passive 4 x 4 matrix (16 key, HC-KP) keypad. Note that the NE64 ports applied may be enabled as EMAC MII signals.

1	PTH0/KWH0
2	PTH1/KWH1
3	PTH2/KWH2
4	PTH3/KWH3
5	PTJ0/KWJ0
6	PTJ1/KWJ1
7	PTJ2/KWJ2
8	PTJ3/KWJ3

This interface is implemented as a software key scan. Pins PTH0-3 are applied as column drivers which are active high outputs. Pins PTJ0-3 are applied for row input and will read high when the keypad key is pressed. Scan software then determines the key number from valid column and row combination.

See the file **`Key12.ASM`** for an example program using this connector.

USER COMPONENTS

The EVB9S12NE64 board provides 4 push button switches (SW1 – 4), 4 buffered LED indicators (LED1 – 4), and a user potentiometer (RV1). All the user components can be applied to dedicated NE64 I/O ports by the USER_EN Switch or RV1_EN option jumper. The user components may be provided for other I/O or application at the USER_IO header also. Use caution and disable USER_EN connections when applying the USER_IO connections to prevent port conflicts.

USER_ENABLE

The USER ENABLE options provide a method to enable or connect the EVB user components applied to the HCS12 I/O ports. The development board user should be familiar with the input and output application so that I/O port conflicts do not occur. Following is the connection reference table:

USER ENABLE POSITION	USER DEVICE	HCS12 I/O PORT	PORT DIRECTION and Active Level	ALTERNATE EVB I/O PORT
1	LED 1	PTG0 / EMAC RXD0	Output, active Low	MII Port, MCU2_GP pin 7
2	LED 2	PTG1 / EMAC RXD1	Output, active Low	MII Port, MCU2_GP pin 8
3	LED 3	PTG2 / EMAC RXD2	Output, active Low	MII Port, MCU2_GP pin 5
4	LED 4	PTG3 / EMAC RXD3	Output, active Low	MII Port, MCU2_GP pin 6
5	SW 1	PTE0 / XIRQ*	Input, active Low	BUS Port, MCU1 pin 33
6	SW 2	PTH4 / EMAC TCLK	Input, active Low	MII Port, MCU2_GP pin 23
7	SW 3	PTH5 / EMAC TXEN	Input, active Low	MII Port, MCU2_GP pin 36
8	SW 4	PTH6 / EMAC TXER	Input, active Low	MCU2_GP pin 25
RV1_EN	RV1 POT	PAD0 / AN0	Input, 0 to 3.3V	MCU2_GP pin 17

NOTE: If the NE64 device EMAC signals are enabled to appear on the device I/O ports, User Enable positions 1 to 9 cannot be applied.

USER_IO Connector

User components maybe applied alternately at the USER-IO connector. Associated USER_EN options should be opened to prevent I/O conflicts when applying this connector.

USER I/O POSITION	USER DEVICE	ACTIVE LEVEL to / from circuit	USER_EN or Option
1	LED 1	Input, active Low	USER_EN Switch 1
2	LED 2	Input, active Low	USER_EN Switch 2
3	LED 3	Input, active Low	USER_EN Switch 3
4	LED 4	Input, active Low	USER_EN Switch 4
5	RV1	Output, 0 – 3.3V	RV1_EN option jumper
6	SW 1	Output active Low	USER_EN Switch 5
7	SW 2	Output active Low	USER_EN Switch 6
8	SW 3	Output, active Low	USER_EN Switch 7
9	SW 4	Output, active Low	USER_EN Switch 8

RV1 User Potentiometer

The User Potentiometer provides an adjustable linear voltage output from 0 to 3.3V. The voltage potential is provided to HCS12 port PAD0 / AN0 by the RV1_EN option jumper being installed on both pins. The HCS12 port PAD0/AN0 should be placed in analog input mode while RV1_EN is installed.

SW1 – SW4 Push Switches

The push switches provide momentary active low input for user applications. Switch idle level of logic 1 or +3.3V is provided by discreet pull-up resistors on the EVB board, internal port pull-ups are not required. SW1 – 4 provide input to HCS12 ports PTE0/XIRQ*, and PTH4 - 6 when USER EN switch positions 5 to 8 are enabled respectfully. Input port PTE0/XIRQ may be configured as the XIRQ interrupt input by clearing the HCS12 X bit in the CCR register with user software. PTH4 – PTH6 provide input interrupt capability also. User should note that the NE64 EMAC MII signals may also be enabled to appear on this port.

LED1 – 4 Indicators

The LED indicators provide an active low output indication for user applications. Indicators are buffered to reduce NE64 device I/O current. LED 1 – 4 are driven from NE64 I/O ports PTG0 – PTG3 respectfully when USER_EN switch positions 1 – 4 are enabled. User should note that the NE64 EMAC MII signals may also be enabled to appear on this port.

BREADBOARD

The Breadboard area provides a convenient and fast interconnection for prototyping circuits on the EVB9S12NE64 board. User may apply 22-24GA solid core wire (stripped) to make connections between the I/O port connectors and the breadboard. Soldering not required.

EVB9S12NE64 PORT CONNECTORS

MCU1_PORT

The MCU1 Port provides access to the MC9S12NE64 I/O ports A, B, E, K and L.

The A, B, E and K I/O ports are also applied as the expanded address and data bus. User should not apply these port pins if the expanded bus is operating.

Port L is also the Ethernet PHY status LED port. User should not apply PTL0 – 4 if Ethernet PHY status indication is being provided.

PB0 / D0	**1**	**2**	PB1 / D1
PB2 / D2	**3**	**4**	PB3 / D3
PB4 / D4	**5**	**6**	PB5 / D5
PB6 / D6	**7**	**8**	PB7 / D7
PA0 / D8	**9**	**10**	PA1 / D9
PA2 / D10	**11**	**12**	PA3 / D11
PA4 / D12	**13**	**14**	PA5 / D13
PA6 / D14	**15**	**16**	PA7 / D15
PK0 / XA14	**17**	**18**	PK1 / XA15
PK2 / XA16	**19**	**20**	PK3 / XA17
PK4 / XA18	**21**	**22**	PK5 / XA19
PK6 / XCS*	**23**	**24**	PK7 / ECS*
PL0	**25**	**26**	PL1
PL2	**27**	**28**	PL3
PL4	**29**	**30**	PL5
PL6	**31**	**32**	GND
PE0 / XIRQ*	**33**	**34**	PE1 / IRQ*
PE2 / R/W*	**35**	**36**	PE3 / LSTRB*
PE4 / ECLK	**37**	**38**	PE5 / MODA
PE6 / MODB	**39**	**40**	PE7

Notes:
1) PA0-7 and PB0-7 are also the Address and Data Bus in Expanded Modes.
2) PK0-7 also provide Expanded Address signals in Expanded Modes with the MODE EMK bit set.
3) PL0-4 provide Ethernet PHY status signals if enabled.
4) PE2-4 provide Data Bus controls in Expanded Modes.

MCU2_GP PORT

The MCU2_GP Port provides access to the M9S12NE64 I/O ports G, H, J, S, T and AD.

The PG0-6, PH0-7, and PJ0-3 I/O ports are also applied as the EMAC MII signals if enabled. User should not apply these port pins if the EMAC MII expansion is operating.

Ports PJ 6 and 7 are also the I2C interface for the EVB EEprom.

PG6 / RXERD0	**1**	**2**	PG7
PG4 / RXCLK	**3**	**4**	PG5 / RXDV
PG2 / RXD2	**5**	**6**	PG3 / RXD3
PG0 / RXD0	**7**	**8**	PG1 / RXD1
VRH	**9**	**10**	VRL
PAD6 / AN6	**11**	**12**	PAD7 / AN7
PAD4 / AN4	**13**	**14**	PAD5 / AN5
PAD2 / AN2	**15**	**16**	PAD3 / AN3
PAD0 / AN0	**17**	**18**	PAD1 / AN1
PE1 / IRQ*	**19**	**20**	RESET*
PS1 / TXD0	**21**	**22**	PS0 / RXD0
PH4 / TCLK	**23**	**24**	EXT_CLK
PH6 / TXER	**25**	**26**	PH5 / TXEN
PJ6 / SDA	**27**	**28**	PJ7 / SCL
PS3 / TXD1	**29**	**30**	PS2 / RXD1
PT6 / IOC6	**31**	**32**	PT7 / IOC7
PT4 / IOC4	**33**	**34**	PT5 / IOC5
PS5 / MOSI	**35**	**36**	PS6 / SCK
PS7 / SS*	**37**	**38**	PS4 / MISO
JP1 - +3.3V	**39**	**40**	GND

Notes:
1) Port G also provides these operations if enabled by option setting:
PG0-6 = MII port signals
PG0-3 = USER LED1-4 .
PG7 = COM1 CTS input.
2) PAD0 = USER RV1 input if optioned.
3) Port S also provides COM1, COM2, IRDA, LCD Port operations.
4) Port H also provides these operations if enabled by option setting:
PH0-5 = MII port signals
PH4-6 = USER SW2-4
.

MII PORT

The MII Port provides access to the M9S12NE64 EMAC I/O if enabled. I/O Ports G0-6, H0-5, and J0-3 should not be applied if the EMAC MII expansion is operating.

JP2 - +3.3V	**1**	**2**	PJ1 / MDIO
PJ0 / MDC	**3**	**4**	PG3 / RXD3
PG2 / RXD2	**5**	**6**	PG1 / RXD1
PG0 / RXD0	**7**	**8**	PG5 / RXDV
PG4 / RXCLK	**9**	**10**	PG6 / RXER
47.5K ohm to GND	**11**	**12**	PH4 / TCLK
PH5 / TXEN	**13**	**14**	PH0 / TXD0
PH1 / TXD1	**15**	**16**	PH2 / TXD2
PH3 / TXD3	**17**	**18**	PJ3 / COL
PJ2 / CRS	**19**	**20**	GND

BDM PORT

The BDM port is a 6 pin header compatible with a Freescale Background Debug Mode (BDM) Pod. This allows the connection of a background debugger for software development, programming and debugging in real-time without using HCS12 I/O resources.

BGND/MODC

1	2 GND
3	4 RESET*
5	6 +3.3V

See the HCS12 Technical Reference Manual for complete documentation of the BDM.

TROUBLESHOOTING

The EVB9S12NE64 is fully tested and operational before shipping. If it fails to function properly, inspect the board for obvious physical damage first. Verify the communications setup as described under GETTING STARTED.

The most common problems are improperly configured communications parameters, and attempting to use the wrong COM port.

1. Verify that your communications port is working by substituting a known good serial device or by doing a loop back diagnostic.

2. Verify the power source, ON/OFF switch is ON, Indicators are ON? You should measure a minimum of 9 volts between the GND and +VIN connections on the TB1 power connector with the standard power supply provided.

3. Disconnect all external connections to the board except for COM1 to the PC and the wall plug power supply.

4. If no power indications, verify the fuse FZ1 is not open. If the +VIN supply is good and the fuse is ok, immediately disconnect power from the board. Contact support@axman.com by email for instructions and provide board name and problem.

5. Make sure that the RESET line is not being held low or the RESET indicator is not lit.

6. Contact support@axman.com by email for further assistance. Provide board name and describe problem.

TABLE 1: LCD Command and Character Codes

Command codes are used for LCD setup and control of character and cursor position. The BUSY flag (bit 7) may be tested before any command updates to verify that any previous command is completed. A read of the command address will return the BUSY flag status and the current display character location address.

Command	Code	Delay
Clear Display, Cursor to Home	**$01**	1.65ms
Cursor to Home	**$02**	1.65ms
Entry Mode:		
Cursor Decrement, Shift off	**$04**	40us
Cursor Decrement, Shift on	**$05**	40us
Cursor Increment, Shift off	**$06**	40us
Cursor Increment, Shift on	**$07**	40us
Display Control:		
Display, Cursor, and Cursor Blink off	**$08**	40us
Display on, Cursor and Cursor Blink off	**$0C**	40us
Display and Cursor on, Cursor Blink off	**$0E**	40us
Display, Cursor, and Cursor Blink on	**$0F**	40us
Cursor / Display Shift: (nondestructive move)		
Cursor shift left	**$10**	40us
Cursor shift right	**$14**	40us
Display shift left	**$18**	40us
Display shift right	**$1C**	40us
Display Function (default 2x40 size)	**$3C**	40us
Character Generator Ram Address set	**$40-$7F**	40us
Display Ram Address and set cursor location	**$80-$FF**	40us

LCD Character Codes

$20	Space	$2D	-	$3A	:	$47	G	$54	T	$61	A	$6E	n	$7B	{
$21	!	$2E	.	$3B	;	$48	H	$55	U	$62	B	$6F	o	$7C	|
$22	“	$2F	/	$3C	{	$49	I	$56	V	$63	C	$70	p	$7D	}
$23	#	$30	0	$3D	=	$4A	J	$57	W	$64	D	$71	q	$7E	>
$24	$	$31	1	$3E	}	$4B	K	$58	X	$65	E	$72	r	$7F	<
$25	%	$32	2	$3F	?	$4C	L	$59	Y	$66	F	$73	s		
$26	&	$33	3	$40	Time	$4D	M	$5A	Z	$67	G	$74	t		
$27	‘	$34	4	$41	A	$4E	N	$5B	[	$68	H	$75	u		
$28	(	$35	5	$42	B	$4F	O	$5C	Yen	$69	I	$76	v		
$29	)	$36	6	$43	C	$50	P	$5D	]	$6A	J	$77	w		
$2A	*	$37	7	$44	D	$51	Q	$5E	^	$6B	K	$78	x		
$2B	+	$38	8	$45	E	$52	R	$5F	¯	$6C	L	$79	y		
$2C	,	$39	9	$46	F	$53	S	$60	`	$6D	M	$7A	z		