DEMO9S12XDT512

DEVELOPMENT BOARD FOR FREESCALE MC9S12XDT512

USER GUIDE

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Revision History

Date	Rev	Comments
March 24, 2005	A	Initial Release
March 31, 2005	B	Added corrections noted in “Out-of-Box” review. Removed reference to serial cable, Demo program and Troubleshooting section.
May 9, 2005	C	Removed Motorola reference in document
August 15, 2005	D	Corrected SCI0 and SCI1 assignments in COM section.
July 18, 2008	E	Updated cover page, removed Appendix B, minor text and formatting corrections

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the DEMO9S12XDT512 board:

   a) This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development module utilizes option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed - jumper is installed such that 2 pins are connected together

Jumper off, out, or idle - jumper is installed on 1 pin only. It is recommended that jumpers be idled by installing on 1 pin so they will not be lost.

Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

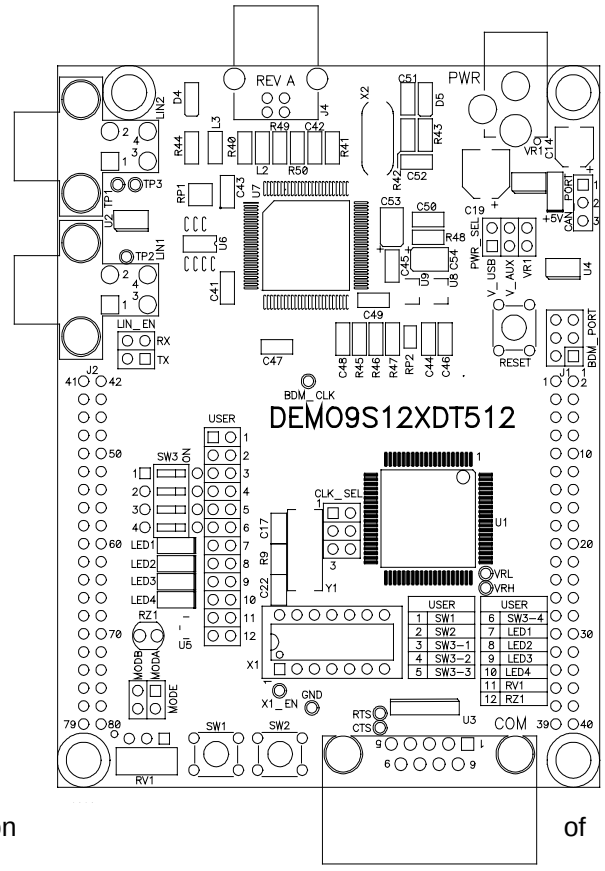
Signal names followed by an asterisk (*) denote active-low signals.

FEATURES

The DEMO9S12XDT512 is an evaluation or demonstration board for the Freescale MC9S12XDT512 MCU. Development of applications is quick and easy with the integrated USB-Multilink BDM, sample software tools, and examples. A standard BDM debug port is also provided, but not populated, to allow use of an external BDM pod. Two 40-pin connectors allow the demonstration board to be connected to an expanded evaluation environment or to external test equipment.

Features:

- MC9S12XDT512 MCU, 80 LQFP
  - X-GATE Co-Processor
  - 512 KB Flash EEPROM
  - 4KB EEPROM
  - 32 KB SRAM
  - 59 GPIO lines
  - Enhanced Capture Timer/PWM
  - SCI and SPI Communications Ports
  - Key Wake-up Port
  - Single Wire BDM Interface
  - CAN 2.0 A/B Module
  - Analog to Digital Converter
  - 80 MHz Bus Operation using internal PLL
- Integrated USB-Multilink BDM for DEBUG access
- Optional power from USB bus through USB-Multilink BDM
- Optional on-board, regulated +5V power supply for stand-alone operation
- Optional power through MCU I/O connector
- Power Input Selection
  - USB Connector
  - 2.0mm barrel connector
  - MCU I/O Connector
- On-Chip Voltage Regulator with low-voltage detect (LVD) and low-voltage interrupt (LVI)
- 4 MHz crystal oscillator in low-power Pierce configuration default
- Optional full-power Pierce configuration (requires installation of R9)
- Socket for optional full- or half-can clock oscillator
- RS-232 serial port w/ DB9 connector
- 8-Ch, 10-bit, ATD with external trigger capability
- 16-Ch, 10-bit, ATD with external trigger capability
- Enhanced Capture Timer with IC, OC, PWM and Pulse Accumulate capabilities
- User Components Provided
  - 4 Position DIP Switch
  - 3 Push Button Switches: 2 User, RESET
  - 7 LED Indicators: 4 User, 2 USB, +5V
- Jumpers
  - Enable/Disable User functions
  - PWR_SEL
  - VX_EN
  - LIN_EN
  - CLK_SEL



- USB_SPEED
- Connectors
  - Two 40-pin, pass-thru type, MCU I/O Connectors, providing access to most MCU IO signals
  - 2.0mm barrel connector power input
  - USB Type-B connector
  - 6-pin BDM interface connector (not installed)
  - DB9 COM connector
  - 2 4-pos LIN connectors
  - 3-pos CAN connector
- Supplied with LIN Cable, USB Cable, Documentation (CD), and Manual

Specifications:
Module Size 4.0" x 3.1"
Power Input: +6VDC to +18VDC
NOTE: LIN functionality supported when powered from PWR connector only

REFERENCES

Reference documents are provided on the support CD in Acrobat Reader format.

DEMO9S12XDT512_UG_A.pdf	DEMO9S12XDT512 User Guide (this document)
DEMO9S12XDT512QSG.pdf	DEMO9S12XDT512 Quick Start Guide
DEMO9S12XDT512 _SCH_D.pdf	DEMO9S12XDT512 Schematic Rev. D
9S12XDP512V2_ZIP.zip	DEMO9S12XDT512 Device User Guide
AN2546.pdf	S12X Load RAM and Execute (LRAE) Program Application Note
AN2615.pdf	HCS12 and S12X Family Compatibility
AN2685.pdf	How to Configure and Use the XGATE on S12X Devices
AN2708.pdf	An Introduction to the External Bus Interface on the HCS12X

GETTING STARTED

To get started quickly, please refer to the DEMO9S12XDT512 Quick Start Guide. This quick start will show the user how to connect the board to the PC, run a LED test program, install the correct version of CodeWarrior Development Studio, and load an Analog to Digital (ATD) test program using CodeWarrior.

OPERATING MODES

The DEMO9S12XDT512 board operates in two operating modes: Run Mode, or Debug Mode. Run Mode allows user application operation from Power-On or Reset. Debug Mode supports the development and debug of applications. See the related sections below for quickly starting the board in the desired operation mode.

The board has been preloaded with a demonstration program. The demo program operates in

the Run Mode. The +5V LED will light when power is applied to the board.

RUN MODE

Run mode allows user application to function when power is applied to the board. Use the following settings to configure the DEMO9S12XDT512 board for RUN Mode to get started quickly.

1. Connect auxiliary equipment to board as required by application.

2. Configure the board option jumpers for run mode.

Table 1: Run Mode Setup

PWR_SEL	Pin1 – Pin2 (VB)
CLK_SEL	Pin1 – Pin2 (Y1)
VX_EN	Off
USER	As Required
LIN_EN	As Required
USB_SPEED	Pin1 – Pin2 (HIGH)

NOTE: See Power section below to configure power input from PWR connector or from J1 connector.

3. Apply power to the board.

4. The programmed application will begin to execute.

Debug Mode

Debug Mode supports application development and debug. Debug mode is available to the user through the integrated USB-Multilink BDM or the by using an external HCS12 BDM cable. Use of the integrated USB-Multilink BDM requires only a host PC with an available USB port and an A/B type USB cable. A 6-pin BDM interface header (BDM_PORT) supports the use of an external HCS12 BDM cable. The BDM_PORT header is not installed in default configuration. The steps below describe using the integrated USB-Multilink BDM.

1. Connect auxiliary equipment to board as required by application.
2. Install and launch P&E PKG12Z tool set, CodeWarrior Development Studio, or other software capable of communicating with the HCS12 MCU.
3. Configure the board option jumpers for DEBUG mode.

Table 2: BDM Mode Setup

PWR_SEL	Pin1 – Pin2 (VB)
CLK_SEL	Pin1 – Pin2 (Y1)
VX_EN	Off
USER	As Required
LIN_EN	As Required
USB_SPEED	Pin1 – Pin2 (HIGH)

NOTE: Refer to the Development Support section below for details on using an external HCS12 BDM cable.

4. Connect the supplied USB cable between an available USB port on the host PC and the USB connector on the board.
5. Hosting development software will establish DEBUG communication.
6. If the P&E Connection Assistant appears, ensure the following settings
   Interface: USB HCS08/HCS12 MULTILINK – USB PORT
   Port: USB1 : USB-ML-12 REF : DEMO9S12XDT512
   CPU: HC12/HCS12 - Autodetect Device Type

MEMORY MAP

The table below shows the default memory map for the MC9S12XDP512 immediately out of reset.

Table 3: Memory Map

$0000 - $07FF	REGISTERS	2 KB	
$0800 - $0FFF	EEPROM	4 KB	4 – 1Kb pages between 0x800 – 0xBFF
$1000 - $3FFF	RAM	12 KB	5 – 4Kb pages between 0x1000 – 0x1FFF
$4000 - $7FFF	FIXED FLASH	16 KB	1K, 2K, 4K, 8K Protected Boot Sector
$8000 - $BFFF	FLASH EEPROM PAGE WINDOW	16 KB	32 – 16Kb pages
$C000 - $EFFF	FIXED FLASH	16 KB	2K, 4K, 8K, 16K Protected Boot Sector
$FF00 - $FFFF	Vectors BDM (if active)	255 bits	

SOFTWARE DEVELOPMENT

Software development will require the use of an assembler or compiler supporting the HCS12 instruction set and a host PC operating a debug interface. The assembler or compiler must also support the HC(S)12 X-Gate instruction set. CodeWarrior Development Studio and Axiom IDE for Windows for Debugging and Flash programming are supplied with this board.

DEVELOPMENT SUPPORT

Application development and debug for the target MC9S12XDT512 is supported through the BDM interface. The BDM interface consists of an integrated USB-Multilink BDM and a 6-pin interface header (BDM_PORT) to connect a HCS12 BDM cable.

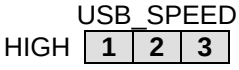
Integrated BDM

The DEMO9S12XDT512 board features an integrated USB-Multilink BDM from P&E Microcomputer Systems. The integrated USB-Multilink BDM supports application development and debugging via background debug mode. All necessary signals are provided by the integrated USB-Multilink BDM. A USB, type B, connector provides connection from the target board to the host PC.

The integrated USB-Multilink BDM provides +5V power and ground to target board eliminating the need to power the board externally. Power from the USB-Multilink BDM is derived from the USB bus; therefore, total current consumption for the target board, and connected circuitry, must not **exceed 500mA**. This current limit describes the current supplied by the USB cable to the BDM, target board, and any connected circuitry. Excessive current drain will violate the USB specification. Damage to the host PC USB hub or the target board may result.

The communications speed over the USB bus is controlled by the USB_SPEED header. When shipped from the factory, the DEMO9S12XDT512 is configured for high-speed operation. If the user encounters a communication failure, USB communication speed may be reduced by setting this option jumper to Full.

Figure 1: USB_SPEED Option Header



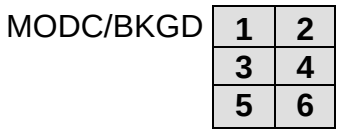
Configuration:
1 – 2: Selects USB High-speed communications
2 – 3: Selects USB Full-speed communications

CAUTION: Do not allow total current drain to **exceed 500mA** when powered from the USB-Multilink BDM .

BDM_PORT Header

A compatible HCS12 BDM cable can also attach to the 6-pin BDM interface header (BDM_PORT). This header is not installed in default configuration. The figure below shows the pin-out for the DEBUG header

Figure 2: BDM_PORT



See the HC12 Reference Manual for complete DEBUG documentation

NOTE: This header is not installed in default configuration.

POWER

The DEMO9S12XDT512 is designed to be powered through the USB-Multilink BDM during application development. A 2.0mm barrel connector has been applied to support stand-alone operation and to support LIN functionality. The board may also be powered through connector J1. This connection may also be used to supply power from the board to external circuitry.

During application development, the board should be configured to draw power from the USB-Multilink BDM. The barrel connector may be used to support LIN functionality during application development. The barrel connector input is also used to provide power during stand-alone operation.

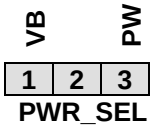
POWER SELECT

Power may be applied to the board through the integrated USB-Multilink BDM circuitry, a 2.0mm barrel connector, or through connector J1. Power selection is achieved using 2 selection headers: PWR_SEL option header and the VX_EN option header.

PWR_SEL

The PWR_SEL option header selects power input either from the integrated USB-Multilink BDM circuitry or from the on-board voltage regulator. The figure below details the PWR_SEL header connections.

Figure 3: PWR_SEL Option Header



CONFIGURATION
1 – 2: Selects power input from USB-ML12
2 – 3: Selects power input from on-board regulator or J1

NOTE: Set PWR_SEL jumper to VB during application development. Use barrel connector input (PWR) to support LIN functionality as needed.

Power from the integrated BDM is drawn from the USB bus and is limited to **500 mA**. This current limit describes the total current supplied over the USB cable to the BDM, target board and any connected circuitry. Current drain in excess of 500 mA will violate the USB specification and may result in damage to the host PC or the target board. At minimum, excessive current drain will cause the host PC to spontaneously reboot. Power is provided through the integrated BDM to the target board.

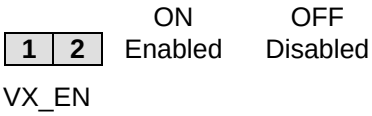
The on-board voltage regulator (VR1) accepts power input through a 2.0mm barrel connector (PWR). Input voltage may range from +6V to +18V. The voltage regulator (VR1) provides a +5V fixed output limited to 250mA. Over-temperature and over-current limit built into the voltage regulator provides protection from excessive stress. Consider the maximum output current limit of VR1 when attempting to power off-board circuitry through connector J1.

VX_EN

The VX_EN option header is a 2-pin jumper that connects/disconnects input J1-1 directly to the target board +5V voltage rail. J1-3 is directly connected to the ground plane. Use of this feature requires a regulated +5V input power source. This power input is decoupled to minimize noise input but is not regulated. Care should be exercised when using this feature; no protection is applied on this input and damage to the target board may result if over-driven. Also, do not attempt to power the target board through this connector while also applying power through the USB-Multilink BDM or the PWR connector; damage to the board may result.

Power may also be sourced to off-board circuitry through the J1 connector. Current output to external circuitry is limited by the current supplied from the USB bus or the on-board regulator. Excessive current drain may damage the target board, the host PC USB hub, or the on-board regulator. The figure below details the VX_EN header connections.

Figure 4. VX_EN Option Header



CAUTION: Do not exceed available current supply from USB-Multilink BDM or on-board regulator, when sourcing power through connector J1 to external circuitry.

RESET SWITCH

The RESET switch provides a method to apply an asynchronous RESET to the MCU. The RESET switch is connected directly to the RESET* input on the MCU. Pressing the RESET switch applies a low voltage level to the RESET* input. A pull-up bias resistor allows normal MCU operation. Shunt capacitance ensures an adequate input pulse width.

LOW VOLTAGE RESET

The MC9S12XDT512 utilizes an internal Low Voltage Reset (LVR) circuit. The LVR holds the MCU in reset until applied voltage reaches an appropriate level. The LVR also protect against under-voltage conditions. Consult the MC9S12XDT512 reference manual for details LVR operation.

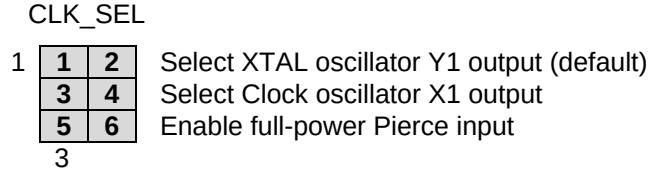
TIMING

Default timing configuration for the DEMO9S12XDT512 is a low-power, low-noise Pierce oscillator. In this mode, oscillator swing is typically $1V_{PP}$. The Pierce oscillator input is supplied by a 4 MHz, fundamental frequency, crystal oscillator at location Y1. The crystal oscillator exhibits a frequency tolerance of 30ppm. An optional socket at X1 is also provided to support alternate MCU input frequencies. This socket supports full- and half-size can clock oscillators.

The XCLKS* signal allows the user to configure the timing input as a full-power Pierce oscillator. Full power Pierce mode requires installing an 0805 size, 1M ohm resistor at location R9. The XCLKS* jumper should be disabled when using an optional clock oscillator.

The CLK_SEL option header selects the on-board XTAL oscillator, the optional CLOCK oscillator socket, or configures the MCU to accept a full-power Pierce Oscillator input as timing source for the MCU. The figure below shows settings for CLK_SEL option header.

Figure 5. CLK_SEL Option Header



NOTE: When applying the Clock Oscillator (X1), do not enable XCLKS*
NOTE: Enabling the full-power Pierce oscillator requires installing a 1M ohm resistor at location R9.

CAUTION: On revision D or earlier boards, only a 3.0V output clock oscillator may be used. Using a clock with 5.0V output will damage the MCU.

COMMUNICATIONS

The DEMO9S12XDT512 board provides two Enhanced Serial Communications Interface (ESCI) ports. SCI0 is applied to RS-232 serial communications (COM) on the target board. SCI1 is applied to LIN communications on the target board. RS-232 communications are supported through a DB9 connector. LIN communications are supported through a pair of 4-pin Molex connectors.

RS-232

An RS-232 translator provides RS-232 to TTL/CMOS logic level translation on the COM connector. The COM connector is a 9-pin Dsub, right-angle connector. A ferrite bead on shield ground provides conducted immunity protection. Communication signals TXD and RXD are routed from the transceiver to the MCU. Hardware flow control signals RTS and CTS are available on the logic side of U3. These signals are routed to vias located near the transceiver (U3). RTS has been biased properly to support 2-wire RS-232 communications.

Communications signals TXD and RXD also connect to general purpose Port S signals.

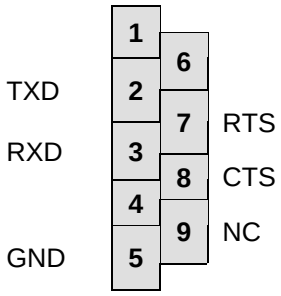
Table 4: COM Connections

MCU Port	COM Signal	I/O PORT CONNECTOR
PS1/TXD	TXD OUT	J1-5
PS0/RXD	RXD IN	J1-7

COM Connector

A standard 9-pin Dsub connector provides external connections for the SCI0 port. The Dsub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. The figure below details the DB9 connector.

Figure 6: COM Connector



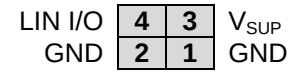
Female DB9 connector that interfaces to the MCU internal SCI0 serial port via the RS232 transceiver. It provides simple 2 wire asynchronous serial communications without flow control. Flow control is provided at test points on the board.

Pins 1, 4, and 6 are connected together.

LIN Communications

The DEMO9S12XDT512 applies the MC33661D Local Interconnect Interface (LIN) physical layer (PHY) for use in developing automotive control applications. The MC33661D physical layer interface (PHY) supports LIN bus functionality for input voltages between +6V and +18V. Only power applied to the PWR connector will enable the LIN bus. Two, 4-pin, Molex connectors provide off-board connectivity. The figure below shows the pin-out of the LIN connector looking into the connector.

Figure 7: LIN Connector



REF: Mating Connector, Molex P/N,
39-01-2040, Housing
39-00-0039, Socket

NOTE: Board must be powered from the PWR connector with V_{IN} between +6V and +18V.

LIN_EN

The LIN_EN option header enables or disables the LIN driver on SCI1.

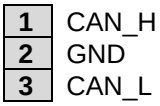
Figure 8. LIN_EN Option Header

NOTE: Board must be powered from the PWR connector with V_{IN} between +6V and 18V.

CAN Communications

The DEMO9S12XDT512 provides a PCA82C250 high-speed CAN physical layer interface (PHY). A 3-pin connector provides connectivity to the off-board CAN bus. The CAN PHY connects to the CAN0 channel on the MCU. The PHY supports data rates up to 1 MBps with edge-rate control to reduce EMI/RFI. The figure below shows the pin-out of the CAN_PORT connector.

Figure 9. CAN_PORT Connector



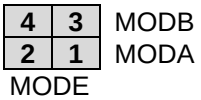
The CAN PHY connects to the CAN0 channel in the MCU

MODE

The MODE option header allows the MCU to be configured between the various modes of operation. Refer to the MC9S12XDP512 Device User Guide for further details on operational modes. Although no external memory is available on the DEMO9S12XDT512 board, external bus signals are available at expansion headers J1 and J2. The figure below shows the settings for the MODE option header. MODE selection status is latched at the rising edge of RESET. An internal pull-down biases the MODA and MODB signals during boot. After RESET, the MODA and MODB signals revert to general-purpose I/O functionality.

The MODE option header is not installed in default configuration. Internal bias configures the MCU for single-chip operation out of reset. To configure the MCU for expanded mode operation, install a 2x2 pin header and install shunts as noted below.

Figure 10. MODE Option Header



	Installed	Removed
MODB	MODB = 1	MODB = 0
MODA	MODA = 1	MODA = 0

NOTE: MODE selection pin status is latched on the rising edge of RESET
NOTE: This header is not installed in default configuration

VRH/VRL

MCU inputs VRH and VRL provide the upper and lower voltage reference for the analog to digital (ATD) converter. By default, VRH is tied to VDD and VRL is tied to ground. Adequate filtering has been added to provide a voltage reference with minimal ripple. Either, or both, references may be isolated to provide alternate ATD input references. A test point via on each signal, labeled VRH, or VRL, provides a convenient attach point.

A 0-ohm configuration resistor allows isolation of each reference voltage. Removing R10 isolates VRH while removing R12 isolates VRL. Install 0805 sized 0-ohm resistors in these locations to restore the board to default configuration.

Care must be exercised when using alternate input references. The associated isolation resistor must be removed before applying an alternate voltage reference or the board may be damaged. The table below summarizes the changes necessary to use alternate VRH and/or VRL.

Table 5: ATD Reference Voltage

	Installed (Default)	Removed
R10	VRH = VDD	VRH provided by user
R12	VRL = GND	VRL provided by user

NOTE: Damage to the board may result if an alternate reference voltage is attached without first removing the associated configuration resistor.

USER I/O

User I/O includes 2 push button switches, one 4-position DIP switch, 4 green LEDs, a potentiometer, and a Light Sensor. The sections below provide details on each User I/O. The User option header block enables or disables each User I/O individually.

SWITCHES

The DEMO9S12XDT512 target board provides 2 push button switches and one 4-position DIP switch for user input. Each push button switch is an active low input with a pull-up resistor bias to prevent indeterminate input conditions. Pressing a push-button switch causes a low logic input on the associated input.

Each DIP switch position is an active low input. Use of the DIP switches requires enabling the associated PORTB pull-ups internal to the MCU prevent indeterminate input conditions. Moving a DIP switch position to ON causes a low logic level on the associated input. The figure below shows the USER enable position and associated signal for each user switch.

LED's

The DEMO9S12XDT512 target board provides 4 green LEDs for output indication. Each LED is an active low output. A series, current-limit resistor prevents excessive diode current. Writing a low logic level to an LED output causes the associated LED to turn on. The figure below shows the USER enable position and associated signal for each user LED.

POT

A single-turn, 3/8 inch, 5K ohm trimmer potentiometer (POT) has been provided as user, analog input. The part is decoupled to minimize noise during adjustment. The POT connects to analog input PAD05/AN05 on the MCU. The figure below shows the USER enable position and associated signal for the potentiometer.

LIGHT SENSOR

A 4mm photocell light sensor exhibiting 23K – 33K ohms of output resistance has been provided. Output resistance is inversely related to incident light intensity. A gain stage (U5) amplifies the sensor output before connecting to the MCU. The SENSOR connects to analog input PAD04/AN04 on the MCU. The figure below shows the USER enable position and associated signal for the Light Sensor

User Signals

The following table shows the connections for each user I/O device.

Table 6: User I/O

USER	Ref Des	Signal	Device
1	SW1	PP0/KWP0/PWM0/MISO1	Push Button Switch
2	SW2	PP1/KWP1/PWM1/MOSI1	Push Button Switch
3	SW3-1	PB0	4-pos DIP Switch
4	SW3-2	PB1	4-pos DIP Switch
5	SW3-3	PB2	4-pos DIP Switch
6	SW3-4	PB3	4-pos DIP Switch
7	LED1	PB4	Green LED
8	LED2	PB5	Green LED
9	LED3	PB6	Green LED
10	LED4	PB7	Green LED
11	RV1	PAD05/AN05	Potentiometer
12	RZ1	PAD04/AN04	Light Sensor

USER ENABLE

The User option header block enables or disables each User I/O device individually. User I/O includes 4 green LEDs, 2 push button switches, one 4-position DIP switch, a Light Sensor, and a potentiometer. Installing a shunt enables the associated option. Removing a shunt disables the associated option. The table below shows the configuration option for each USER I/O.

Table 7: USER Option Header

	USER		Shunt Installed	Shunt Removed	Description
SW1	**1**	**2**	Enable	Disable	Push Button Switch 1
SW2	**3**	**4**	Enable	Disable	Push Button Switch 2
SW3-1	**5**	**6**	Enable	Disable	DIP Switch Position 1
SW3-2	**7**	**8**	Enable	Disable	DIP Switch Position 2
SW3-3	**9**	**10**	Enable	Disable	DIP Switch Position 3
SW3-4	**11**	**12**	Enable	Disable	DIP Switch Position 4
LED1	**13**	**14**	Enable	Disable	LED 1
LED2	**15**	**16**	Enable	Disable	LED 2
LED3	**17**	**18**	Enable	Disable	LED 3
LED4	**19**	**20**	Enable	Disable	LED 4
RV1	**21**	**22**	Enable	Disable	Potentiometer
RZ1	**23**	**24**	Enable	Disable	Light Sensor

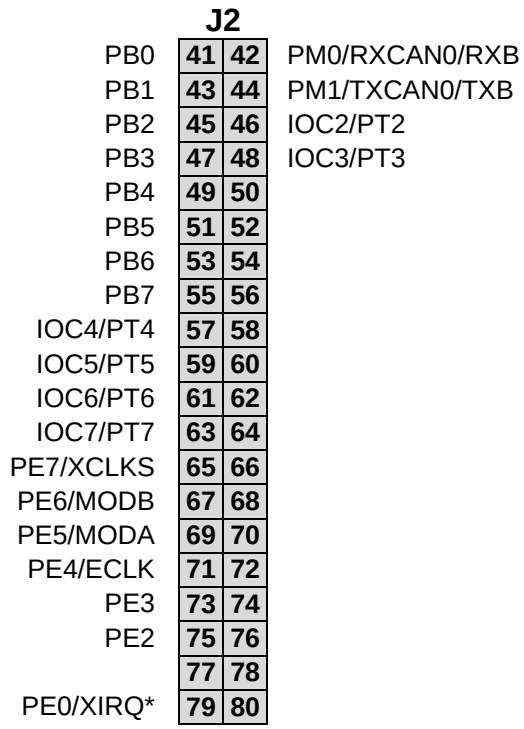
MCU I/O PORT

The MCU I/O PORT connectors (J1 and J2) provide access to the MC9S12XDT512 I/O signals. The figures below show the pin-out for each MCU I/O connector.

Figure 11: MCU I/O PORT – J1

	J1		
VDD	**1**	**2**	IRQ/PE1
VSS	**3**	**4**	RESET*
PS1/TXD0	**5**	**6**	MODC/BKGD
PS0/RXD0	**7**	**8**	PP7/KWP7/PWM7/SCK2
PP0/KWP0/PWM0/MISO1	**9**	**10**	PAD07/AN07
PP1/KWP1/PWM1/MOSI1	**11**	**12**	PAD06/AN06
PT0/I0C0	**13**	**14**	PAD05/AN05
PT1/IOC1	**15**	**16**	PAD04/AN04
PM4/RXCAN2/RXCAN0/RXCAN4/MOSI0	**17**	**18**	PAD03/AN03
PM2/RXCAN1/RXCAN0/MISO0	**19**	**20**	PAD02/AN02
PM5/TXCAN2/TXCAN0/TXCAN4/SCK0	**21**	**22**	PAD01/AN01
PM3/TXCAN1/TXCAN0/SS0	**23**	**24**	PAD00/AN00
PA7	**25**	**26**	PJ6/KWJ6/RXCAN4/SDA0
PA6	**27**	**28**	PJ7/KWJ7/TXCAN4/SCL0
PA5	**29**	**30**	PP2/KWP2/PWM2/SCK1
PA4	**31**	**32**	PP3/KWP3/PWM3/SS1
PA3	**33**	**34**	PP4/KWP4/PWM4/MISO2
PA2	**35**	**36**	PP5/KWP5/PWM5/MOSI2
PA1	**37**	**38**	PS2/RXD1
PA0	**39**	**40**	PS3/TXD1

Figure 12. MCU I/O PORT – J2



APPENDIX A

Top Silkscreen