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DEMO9S08LH64

Demonstration Board for Freescale MC9S08LH64 Microcontroller

also applies to MC9S08LL64 Microcontroller

USER GUIDE

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CONTENTS

CAUTIONARY NOTES **4**
TERMINOLOGY **4**
FEATURES **5**
REFERENCES **6**
GETTING STARTED **6**
MEMORY MAP **6**
SOFTWARE DEVELOPMENT **7**
DEVELOPMENT SUPPORT **7**
INTEGRATED BDM 7
BDM OPTION HEADERS *8*
BDM_PORT HEADER 8
POWER **8**
POWER SELECT 9
V_SEL *9*
VDD_EN *10*
VX_EN *10*
JP3 OPTION HEADER 11
RESET SWITCH **11**
LOW VOLTAGE RESET **11**
TIMING **11**
COMMUNICATIONS **12**
USB SERIAL LINK 12
RS-232 12
COM CONNECTOR *12*
COM_SEL *13*
LCD **13**
USER I/O **13**
BUZZER *13*
POTENTIOMETER *14*
LIGHT SENSOR *14*
VDD1 ENABLE *14*
PUSHBUTTON SWITCHES *14*
USER LED'S *15*
MCU I/O PORT **16**

FIGURES

Figure 1: Memory Map....6
Figure 2: JP1 Option Header....8
Figure 3: JP2 Option Header....8
Figure 4: BDM_PORT Header....8
Figure 5: V_SEL Option Header....9
Figure 6: VDD_EN Option Header....10
Figure 7: VX_EN Option Header....11
Figure 8: JP3 Option Header....11
Figure 9: COM Connections....12
Figure 10: COM Connector....12
Figure 11: COM_SEL Option....13
Figure 12: User1 Option Header....14
Figure 13: User2 Option Header....15
Figure 14: User3 Option Header....15
Figure 15: MCU I/O PORT – J1....16

REVISION

Date	Rev	Comments
February 6, 2009	A	Initial Release

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the DEMO9S08LH64 board:

   a) This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development module utilizes option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

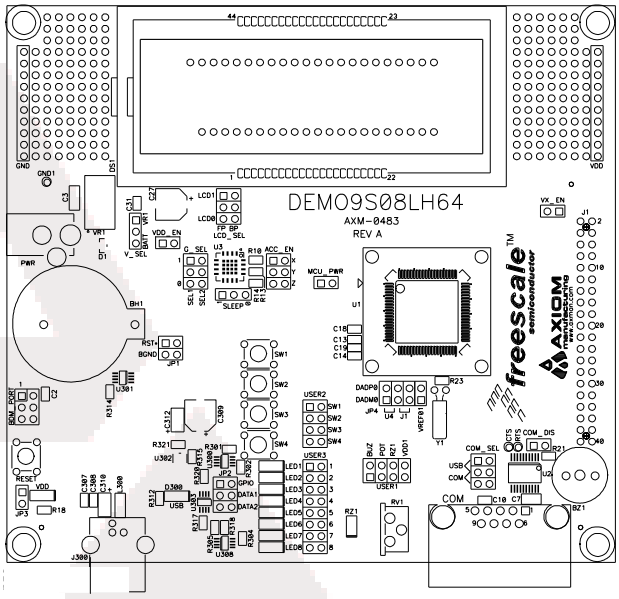
Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Signal names followed by an asterisk (*) denote active-low signals.

FEATURES

The DEMO9S08LH64 is a demonstration board for the MC9S08LH64 microcontroller. Application development is quick and easy with the integrated USB-BDM, sample software tools, and examples. An optional BDM_PORT port is also provided to allow use of a BDM_PORT cable. Two, 40-pin connectors provide access to all IO signals on the target MCU.

All references to DEMO9S08LH64 also apply to DEMO9S08LL64.



- MC9S08LH64, MC9S08LL64, 80LQFP
  - 64K Bytes Flash
  - 4K Bytes RAM
  - Internal Oscillator
  - Integrated LCD Driver
  - 10 MHz Bus Frequency
- Integrated P&E USB-BDM
- BDM_PORT header for BDM cable support (not installed)
- MCU_PORT socket header for access to MCU IO signals
- On-board +5V regulator
- Battery holder for Li-ion battery
- Optional Power from USB-BDM or MCU_PORT connector
- Power Input Selection Jumpers
  - Power input from USB-BDM
  - Power input from on-board regulator
  - Power from battery holder, CR2325
  - Power input from Connector J1
  - Optional Power output through Connector J1
- User Components Provided
  - 5 Push Switches; 4 User, 1 Reset
  - 10 LED Indicators; 8 User, VDD, USB
  - 5K ohm POT w /LP Filter
  - Light Sensor w/ LP Filter and Op Amp
- User Option Jumpers to disconnect Peripherals
- Connectors
  - 40-pin MCU I/O Connector
  - 2.0mm Barrel Connector
  - BDM_PORT (not installed)
  - USB Connector
  - DB9 Connector

Specifications:
Board Size 5.25” x 4.80”
Power Input: +9V typ, +6V min

REFERENCES

Reference documents are provided on the support CD in Acrobat Reader format.

DEMO9S08LH64_UG.pdf	DEMO9S08LH64 User Guide (this document)
DEMO9S08LH64_QSG.pdf	DEMO9S08LH64 Quick Start Guide
DEMO9S08LH64 _SCH_A.pdf	DEMO9S08LH64 Schematic Rev. A
DEMO9S08LH64_Silk_A.pdf	DEMO9S08LH64 Top Silk, Rev A
DEMO9S08LL64 _SCH_A.pdf	DEMO9S08LL64 Schematic Rev. A
DEMO9S08LL64_Silk_A.pdf	DEMO9S08LL64 Top Silk, Rev A
DEMOLL_LH_TEST.zip	CW LCD Demo Program Source Code

GETTING STARTED

To get started quickly, please refer to the DEMO9S08LH64 Quick Start Guide. This quick start will illustrate connecting the board to a PC, installing the correct version of CodeWarrior Development Studio, and running a simple LCD test program.

MEMORY MAP

The table below shows the CPU address memory map for the MC9S08LH64 immediately out of reset. Refer to the MC9S08LH64 Data Sheet (DS) for further information.

Figure 1: Memory Map

$0000 - $005F	Direct Page Registers	96 bytes
$0060 - $0F7F	RAM	4000 bytes
$1000 - $103B	LCD Registers	60 bytes
$103C - $17FF	Unimplemented	39,208 bytes
$1800 - $18A0	High Page Registers	160 bytes
$18A1 - $3FFF	Reserved	10,079 bytes
$4000 - $4FFF	Reserved PPAGE = 1	See MPU Reference Manual for details
$5000 - $5FFF	FLASH	12,288 bytes
$8000 - $BFFF	Paging Window PPAGE + A[13:0]	See MPU Reference Manual for details
$E000 - $FFFF	FLASH PPAGE = 3	16,384 bytes

SOFTWARE DEVELOPMENT

Software development requires the use of a compiler or an assembler supporting the HCS08 instruction set and a host PC operating a debug interface. CodeWarrior Development Studio for Microcontrollers is supplied with this board for application development and debug.

DEVELOPMENT SUPPORT

Application development and debug for the target MC9S08LH64 is supported through the background debug mode (BDM) interface. The BDM interface consists of an integrated USB-Multilink BDM and a 6-pin interface header (BDM_PORT). The BDM_PORT header allows connecting a HCS12/HCS08 BDM cable.

Integrated BDM

The DEMO9S08LH64 board features an integrated USB-Multilink BDM from P&E Microcomputer Systems. The integrated USB-Multilink BDM supports application development and debugging via background debug mode. All necessary signals are provided by the integrated USB-Multilink BDM. A USB, type B, connector provides connection from the target board to the host PC.

The integrated USB-Multilink BDM provides power and ground to target board eliminating the need to power the board externally. Power from the USB-Multilink BDM is derived from the USB bus; therefore, total current consumption for the target board, and connected circuitry, **must not exceed 500mA**. This current limit describes the current supplied by the USB cable to the BDM circuit, the target board, and any connected circuitry. Excessive current drain will violate the USB specification causing the bus to disconnect. Damage to the host PC USB hub or the target board may result.

CAUTION:

When powered from the USB bus, do not exceed the 500mA maximum allowable current drain. Damage to the target board or host PC may result

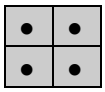
NOTE:

10K ohm pull-ups are applied to BDM signals RESET* and BKGD inside the P&E BDM block

BDM OPTION Headers

Option headers at JP1 and JP2 connect the integrated BDM to the target board. Option header JP1 connects signals RST* and BGND to the target MCU.

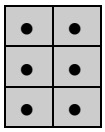
Figure 2: JP1 Option Header



RST*	Connects BDM RESET* to target MCU
BGND	Connects BDM BGND to target MCU

Option header JP2 connects two timer channels to the BDM to facilitate the Signal Analyzer functionality.

Figure 3: JP2 Option Header

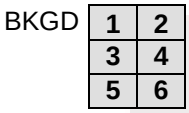


GPIO	GPIO signal to BDM to ensure connectivity
DATA1	Timer channel 0 input to Signal Analyzer
DATA2	Timer channel 1 input to Signal Analyzer

BDM_PORT Header

A compatible HCS12 BDM cable can also attach to the 6-pin BDM interface header (BDM_PORT). This header is not installed in default configuration. The figure below shows the pin-out for the DEBUG header. This information is included for completeness.

Figure 4: BDM_PORT Header



See the MC9S08LH64 Data Sheet for complete DEBUG documentation

NOTE: This header is not installed in default configuration.

POWER

The DEMO9S08LH64 provides several methods to apply power to the board. An option header allows selection between the various power inputs. For application development and debug, the board may be powered from the USB BDM. The 2.0mm PWR connector supports stand-alone operation and higher power requirements. A 190mAH battery holder is applied for low-power operation. Power may also be applied to connector J1 or the board may be configured to supply power from connector J1 to external circuitry.

CAUTION:

Damage to the board may result if voltages greater than +3.3V are applied to the connector J1 input.

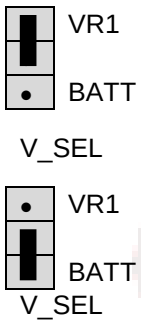
POWER SELECT

Power may be applied to the board through the integrated USB-Multilink BDM circuitry, a 2.0mm barrel connector, from the battery holder, or through connector J1. Power selection is achieved using 2 selection headers: the V_SEL option header and the VX_EN option header.

V_SEL

The V_SEL option header allows the user to select power input either from any of the various input sources. When the VDD_EN option jumper is removed, the RST* and BGND option jumpers should also be removed, to ensure proper operation. The figure below details the PWR_SEL header connections.

Figure 5: V_SEL Option Header



Enables voltage input from on-board regulator. This option should be selected when powered from an external power source connected to PWR connector or powered from the integrated BDM

Enables voltage input from battery holder. This option should be selected when battery-powered operation is desired

Power from the integrated BDM is drawn from the USB bus and is limited to **500 mA**. This current limit accounts for the total current supplied over the USB cable to the BDM circuit, the target board, and any connected circuitry. Current drain in excess of 500 mA will violate the USB specification and will cause the USB bus to disconnect. This will cause the board to exhibit power cycling where the board appears to turn-on then off continually. Damage to the host PC or the target board may also result.

The on-board voltage regulator (VR1) accepts power input through a 2.0mm barrel connector (PWR). Input voltage may range from +5V to +35V; however, input voltage should be limited to prevent the voltage regulator (VR1) from overheating. VR1 provides a +3.3V fixed output limited to 500mA. Over-temperature and over-current limit built into the voltage regulator provides protection from excessive stress. The user should consider the maximum output current limit of VR1 when attempting to power off-board circuitry through connector J1.

To power the board externally while using the integrated BDM for debugging, simply connect an external power source to the PWR connector. Voltage input **must** be greater than +5V. Voltage output from the BDM is diode OR'd to the PWR connector then routed to the on-board regulator. Connecting an input voltage less than +5V to the PWR connector may damage the target board.

Caution:

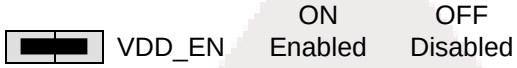
External voltage greater than +5V **must** be applied if powering the board externally while using the integrated BDM for debugging. This is required to overcome the OR'ing diode V_F.

The battery holder at BATT accepts a 3.3V, 23mm, 190mAH lithium-ion battery.

VDD_EN

The VDD_EN option header enables and disables VDD to the target board peripherals. Power to the MCU is unaffected by this option jumper. Removing this option jumper, along with others, allows the user to take accurate MCU current measurements. The figure below shows the VDD_EN option jumper connections.

Figure 6: VDD_EN Option Header



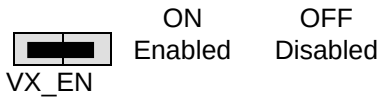
NOTE: If VDD_EN option jumper is OFF, then RST* and BGND option jumpers should also be OFF to ensure proper MCU operation.

VX_EN

The VX_EN option header is a 2-pin jumper that connects or disconnects input J1-1 directly to the target board voltage rail. J1-3 is directly connected to the ground plane. Use of this feature requires a regulated input power source. This power input is decoupled to minimize noise but is not regulated. Care should be exercised when using this feature; no protection is applied on this input and damage to the target board may result if over-driven. Also, do not attempt to power the target board through this connector while also applying power through the USB-Multilink BDM or the PWR connector; damage to the board may result.

Power may also be sourced to off-board circuitry through the J1 connector. The current supplied from the USB bus or the on-board regulator limits current available to external circuitry. Excessive current drain may damage the target board, the host PC USB hub, or the on-board regulator. The figure below details the VX_EN header connections.

Figure 7: VX_EN Option Header



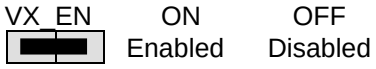
CAUTION:

Do not exceed available current supply from USB-BDM or on-board regulator when sourcing power through connector J1 to external circuitry.

JP3 OPTION HEADER

Option header JP3 enables and disables the VDD LED. This jumper is useful to remove external power drains when attempting MCU current measurements. Use of this option jumper does not affect VDD. The figure below shows the JP3 option header connections.

Figure 8: JP3 Option Header



NOTE: Use of the JP3 option header does not affect VDD.

RESET SWITCH

The RESET switch applies an asynchronous RESET to the MCU. The RESET switch is connected directly to the RESET* input on the MCU. Pressing the RESET switch applies a low voltage level to the RESET* input. A pull-up bias resistor allows normal MCU operation. Shunt capacitance ensures an adequate input pulse width.

LOW VOLTAGE RESET

The MC9S08LH64 utilizes an internal Low Voltage Detect (LVD) circuit. The LVD holds the MCU in reset until applied voltage reaches an appropriate level. The LVD also protect against under-voltage conditions. Consult the MC9S08LH64 reference manual for details LVD operation.

TIMING

The DEMO9S08LH64 internal timing source is active from RESET by default. An external 32 kHz XTAL oscillator, configured for low-power operation, is also provided. Refer to the MC9S08LH64 Data Sheet for details on configuring the selected timing source.

COMMUNICATIONS

The DEMO9S08LH64 supports serial communications through the integrated USB-BDM and an on-board, low-voltage, RS-232 transceiver. The transceiver provides valid RS-232 signaling for input voltage levels down to +1.8V. The COM_SEL header selects the serial path applied.

USB SERIAL LINK

The integrated USB-BDM provides a serial link from the target MCU to the host PC through the host application. Refer to the P&E Multilink documentation for further details.

RS-232

An RS-232 translator provides RS-232 to TTL/CMOS logic level translation on the COM connector. The COM connector is a 9-pin Dsub, right-angle connector. A ferrite bead on shield ground provides conducted immunity protection. Communication signals TXD1 and RXD1 are routed from the transceiver to the MCU. Hardware flow control signals RTS and CTS are available on the logic side of the transceiver. These signals are routed to vias located near the transceiver. RTS has been biased properly to support 2-wire RS-232 communications.

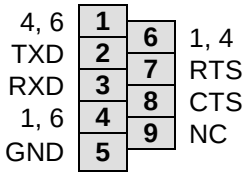
Figure 9: COM Connections

MCU Port	COM Signal	I/O PORT CONNECTOR
PTC1/TXD	TXD	J1-5
PTC0RXD	RXD	J1-7

COM Connector

A standard 9-pin Dsub connector provides external connections for the SCI0 port. The Dsub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. The figure below details the DB9 connector.

Figure 10: COM Connector



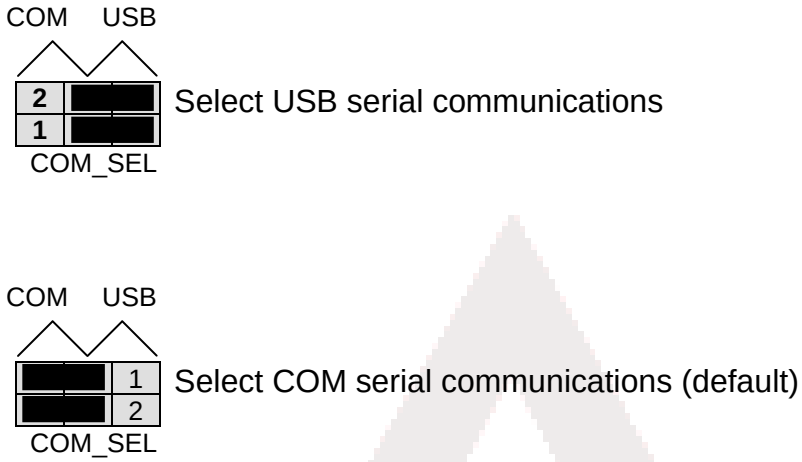
Female DB9 connector that interfaces to the MCU internal SCI0 serial port via the RS232 transceiver. Flow control is provided at test points on the board.

Pins 1, 4, and 6 are connected together.

COM_SEL

The COM_SEL option header connects the MCU SCI port to either the SCI PHY or the USB-BDM connection.

Figure 11: COM_SEL Option



LCD

The DEMO9S08LH64 applies a GD-5663P, 8x36 LCD glass connected directly to the target MCU. The target MCU provides internal charge-pump and regulated LCD reference. The LCD contrast is trimmable under MCU control. Refer to the MC9S08LH64 Reference Manual for further details on using the LCD interface. The GD-5663P datasheet may be found on the Support CD included with the board.

USER I/O

User I/O includes 1 potentiometers, 1 Light Sensor, 2 push button switches, and 2 green LEDs for user I/O. The User option header block enables or disables each User I/O function individually.

Buzzer

The DEMO9S08LH64 target board provides an externally modulated piezo-buzzer for audible applications. A push-pull drive circuit allows the target MCU to easily drive the buzzer at a center frequency of 2300 Hz. Figure 12: below shows the USER enable position and associated signal for the buzzer.

Potentiometer

The DEMO9S08LH64 target board provides a 5K ohm potentiometer (POT) to simulate analog input. The POT is decoupled to minimize noise during adjustment. The figure below shows the USER enable position and associated signal for the potentiometer. Figure 12: below shows the USER enable position and associated signal for the buzzer.

Light Sensor

A surface-mount phototransistor, at RZ1, provides light sensitive, variable input for user applications. Current flow within the phototransistor is inversely proportional to light intensity incident on the surface of the device. A rail-to-rail OP amp at U5 boosts the photocell output to useable levels. Figure 12: below shows the USER enable position and associated signal for the buzzer.

VDD1 Enable

The VDD1 option jumper disconnects the POT, BUZZER, and Light sensor from board power for low-power operation. Figure 12: below shows the USER enable position and associated signal for the buzzer.

Figure 12: User1 Option Header

USER1		Signal	ON	OFF
• •	Buzzer	PTC2/TPM1CH0	Enabled	Disabled
• •	POT	PTA0/KBIP0/ADP0	Enabled	Disabled
• •	RZ1	PTA6/ADP6	Enabled	Disabled
• •	VDD1	VDD	Enabled	Disabled

CAUTION:

Do not enable POT and SW3 at the same time. The POT and SW3 share a common MCU signal input. Pressing SW3 while the POT is rotated to maximum will cause a VDD –GND short. Damage to the board may result.

Pushbutton Switches

The DEMO9S08LH64 provides 4 push-button switches for user input. Each push-button switch is configured for active-low operation. No bias is applied to these push-button inputs. Use of target MCU internal pull-ups is required for proper operation. Figure 13 below shows the USER enable position and associated signal for each user switch.

Figure 13: User2 Option Header

USER2		Signal	ON	OFF
•	• SW1	PTA6/KBIP6	Enabled	Disabled
•	• SW2	PTA7/KBIP7	Enabled	Disabled
•	• SW3	PTA0/KBIP0	Enabled	Disabled
•	• SW4	PTB6	Enabled	Disabled

CAUTION:

Do not enable POT and SW3 at the same time. The POT and SW3 share a common MCU signal input. Pressing SW3 while the POT is rotated to maximum will cause a VDD –GND short. Damage to the board may result.

User LED's

The DEMO9S08LH64 target board provides 8, green, LEDs for output indication. Each LED is configured for active-low operation. A series, current-limit resistor prevents excessive diode current. Figure 14 below shows the USER enable position and associated signal for each user LED.

Figure 14: User3 Option Header

USER3		Signal	ON	OFF
•	• LED1	PTC2/TPM1CH0	Enabled	Disabled
•	• LED2	PTC3/TPM1CH1	Enabled	Disabled
•	• LED3	PTC4/TPM2CH0	Enabled	Disabled
•	• LED4	PTC5/TPM2CH1	Enabled	Disabled
•	• LED5	PTB4	Enabled	Disabled
•	• LED6	PTB5	Enabled	Disabled
•	• LED7	PTB6	Enabled	Disabled
•	• LED8	PTB7	Enabled	Disabled

NOTE:

SW4 and LED7 share a common MCU signal input. If both components are enabled, then pressing SW4 will cause LED7 to light regardless of firmware application function

NOTE:

SW1 and RZ1 share a common MCU signal input. If both components are enabled at the same time, SW 1 may not function properly.

MCU I/O PORT

The MCU I/O PORT connectors (J1 and J2) provide access to the MC9S08LH64 I/O signals. The figures below show the pin-out for each MCU I/O connector.

Figure 15: MCU I/O PORT – J1

VDD	1	2	PTC7/IRQ/TCLK
VSS	3	4	PTB2/RESET*
PTC1/TXD	5	6	PTC6/ACMPO/BKGD/MS
PTC0/RXD	7	8	PTA0/SS*/KBIP0/ADP0
PTC4/TPM2CH0	9	10	PTA1/SPSCK/KBIP1/ADP1
PTC5/TPM2CH1	11	12	PTA2/MISO/SDA/KBIP2/ADP2
PTC2/TMP1CH0	13	14	PTA3/MOSI/SCL/KBIP3/ADP3
PTC3/TPM1CH1	15	16	
PTB5/MOSI/SCL	17	18	
PTB4/MISO/SDA	19	20	PTA6/KBIP6/ADP6/ACMP+
PTB6/SPSCK	21	22	PTA7/KBIP7/ADP7/ACMP-
PTB7/SS*	23	24	
	25	26	
DADP0	27	28	
DADM0	29	30	PTA2/MISO/DSA/KBIP2/ADP2
VREF01	31	32	PTA3/MOSI/SCL/KBIP3/ADP3
	33	34	VSS
VDD	35	36	VSS
VSS	37	38	VDD
VLCD	39	40	VDD