DOC-0469-010, REV D

DEMO9S08LG32

Demonstration Board for Freescale MC9S08LG32 Microcontroller

USER GUIDE

AXIOM manufacturing

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REVISION

Date	Rev	Comments
November 21, 2008	A	Initial Release
December 02, 2008	B	Updated DEMO9S08LG32 connector pins, features, MCU I/O port, and demonstration board diagram.
February 24, 2009	C	Minor updates to format and corrections to content . Added Notes and Caution boxes
April 7, 2009	D	Updated COM_SEL header silk text. Corrected description of JP3 Option header

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the DEMO9S08LG32 board:

   a) This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development module utilizes option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

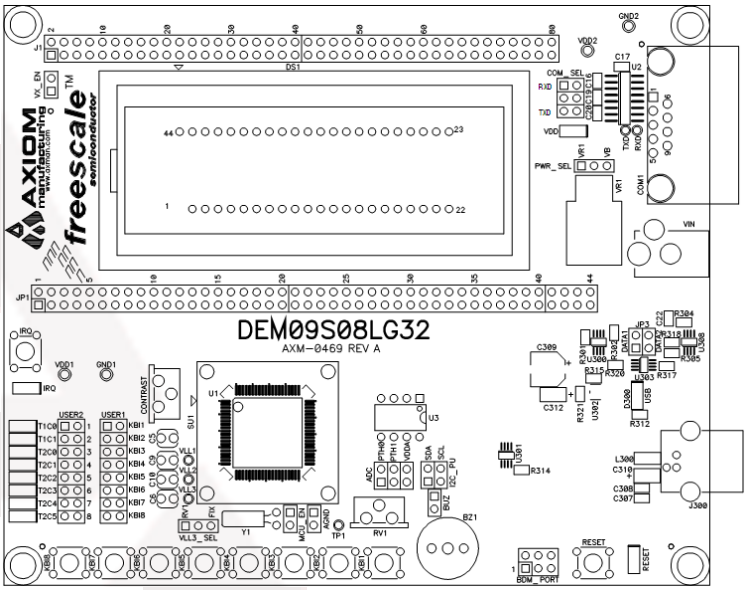
Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Signal names followed by an asterisk (*) denote active-low signals.

FEATURES

The DEMO9S08LG32 is a demonstration board for the MC9S08LG32 microcontroller. Application development is quick and easy with the integrated USB-BDM, sample software tools, and examples. An optional BDM_PORT port is also provided to allow use of a BDM_PORT cable. One, 80-pin connector provides access to all IO signals on the target MCU.



- MC9S08LG32, 80 LQFP
  - 32K Bytes Flash
  - 2K Bytes RAM
  - Internal Oscillator
- On-Board 4x40 Custom LCD Glass
- Integrated P&E USB-BDM
- BDM_PORT header for BDM cable support
- MCU_PORT pin header for access to MCU IO signals
- On-board +5V regulator
- Optional Power from USB-BDM or MCU_PORT connector
- Power Input Selection Jumpers
  - Power input from USB-BDM
  - Power input from on-board regulator
  - Power input from Connector J1
  - Optional Power output through Connector J1
- User Components Provided
  - 10 Push Switches; 8 User, 1 Reset, 1 IRQ
  - 12 LED Indicators; 8 User, VDD, IRQ, USB, and reset
  - 5K ohm POT w /LP Filter for ADC input
  - LCD Glass Contrast POT
  - 2.3kHz Piezo Buzzer
- User Option Jumpers to disconnect Peripherals
- User Option Jumpers to disconnect LCD Signals
- Connectors
  - 80-pin MCU I/O Pin Header
  - 2.0mm Barrel Connector
  - BDM_PORT Connector for External BDM Cable
  - USB Connector
  - DB9 Connector (not installed)

Specifications:
Board Size 5.5” x 4.5”

NOTE:

Manual LCD contrast control requires +12V power input at VIN barrel connector.

REFERENCES

Reference documents are provided on the Axiom Support web site Acrobat Reader format. These documents may be accessed at www.axman.com/support.

DEMO9S08LG32_UG.pdf	DEMO9S08LG32 User Guide (this document)
DEMO9S08LG32 _SCH_A.pdf	DEMO9S08LG32 Schematic Rev. A
DEMO9S08LG32_Silk_A.pdf	DEMO9S08LG32 Top Silk, Rev A
AppsDemo.s19	CodeWarrior LCD Demo Program Object Code

MEMORY MAP

The table below shows the default memory map for the MC9S08LG32 immediately out of reset. Refer to the MC9S08LG32 Data Sheet (DS) for further information.

Figure 1: Memory Map

$0000 - $005F	Direct Page Registers
$0060 - $081F	RAM 1980 Bytes
$0820 - $085C	LCD Registers
$0860 - $17FF	Unimplemented
$1800 - $187A	High Page Registers
$187B - $7FFF	Unimplemented
$8000 - $BFFF	FLASH A
$C000 - $FFFF	FLASH B

SOFTWARE DEVELOPMENT

Software development requires the use of a compiler or an assembler supporting the HCS08 instruction set and a host PC operating a debug interface. CodeWarrior Development Studio for Microcontrollers is supplied with this board for application development and debug. Refer to the supporting CodeWarrior documentation for details on use and capabilities.

DEVELOPMENT SUPPORT

Application development and debug for the target MC9S08LG32 is supported through the background debug mode (BDM) interface. The BDM interface consists of an integrated USB-Multilink BDM and a 6-pin interface header (BDM_PORT). The BDM_PORT header allows connecting a HCS12/HCS08 BDM cable.

Integrated BDM

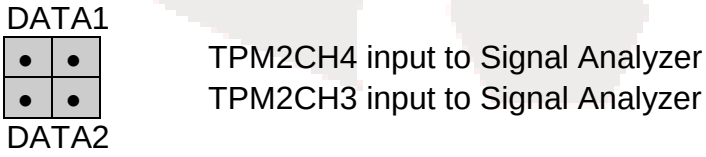
The DEMO9S08LG32 board features an integrated USB-Multilink BDM from P&E Microcomputer Systems. The integrated USB-Multilink BDM supports application development and debugging via background debug mode. All necessary signals are provided by the integrated USB-Multilink BDM. A USB, type B, connector provides connection from the target board to the host PC.

The integrated USB-Multilink BDM provides power and ground to the target board eliminating the need to power the board externally. Power from the USB-Multilink BDM is derived from the USB bus; therefore, total current consumption for the target board, and connected circuitry, **must not exceed 500mA**. This current limit describes the current supplied by the USB cable to the BDM circuit, the target board, and any connected circuitry. Excessive current drain will violate the USB specification causing the bus to disconnect. Damage to the host PC USB hub or the target board may result.

USB-BDM OPTION Headers

Option header JP3 connects two timer channels to the USB-BDM to facilitate the Signal Analyzer functionality. Installing an option jumper shunt enables the selected timer channel to the BDM circuitry.

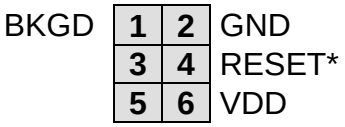
Figure 2: JP3 Option Header



BDM_PORT Header

A compatible HCS12 BDM cable may also attach to the 6-pin BDM interface header (BDM_PORT). Figure 3 below shows the pin-out for the BDM_PORT header.

Figure 3: BDM_PORT Header



Refer to MC9S08LG32 Reference Manual complete for details

POWER

The DEMO9S08LG32 uses several methods to apply power to the board. An option header allows selection between the various power inputs. For application development and debug, the board may be powered from the USB BDM. The 2.0mm, center-positive, barrel connector (VIN) supports stand-alone operation and higher power requirements. Power may also be applied to connector J1 or the board may be configured to supply power from connector J1 to external circuitry.

CAUTION:

Damage to the board may result if voltages greater than +5.5V are applied at the connector J1 input.

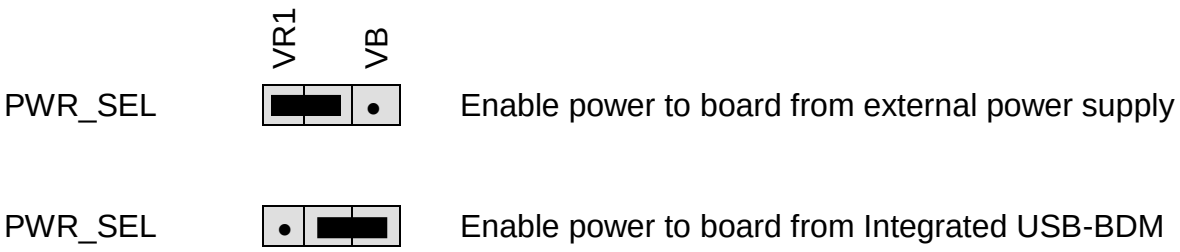
POWER SELECT

Power may be applied to the board through the integrated USB-Multilink BDM circuitry, a 2.0mm barrel connector, or through connector J1. Power selection is achieved using 2 selection headers: the PWE_SEL option header and the VX_EN option header.

PWR_SEL

The PWR_SEL option header allows the user to select power input either from either an external power source connected to the VIN connector or from the integrated USB-BDM. Figure 4 below details the PWR_SEL header connections.

Figure 4: V_SEL Option Header



CAUTION:

Total power from the USB-BDM is limited to **500 mA**. Exceeding this limit violates the USB specification and will cause the USB bus to disconnect. Damage to the target board and the host PC may result.

Power from the integrated BDM is drawn from the USB bus and is limited to **500 mA**. This current limit accounts for the total current supplied over the USB cable to the BDM circuit, the target board, and any connected circuitry. Current drain in excess of 500 mA will violate the USB specification and will cause the USB bus to disconnect. This will cause the board to exhibit power cycling where the board appears to turn-on then off continually. Damage to the host PC or the target board may also result.

Power input to the VIN barrel connector should not exceed +12V. LCD contrast is connected directly to the VIN power input.

CAUTION:

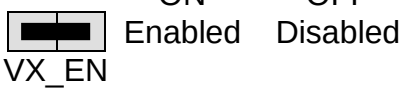
Voltage input exceeding +12V applied to VIN may damage the target board

VX_EN

The VX_EN option header is a 2-pin jumper that connects or disconnects input J1-1 directly to the target board voltage rail. J1-3 connects directly to the target board ground plane. Use of this feature requires a regulated input power source. This power input is decoupled to minimize noise but is not regulated or protected. Care should be exercised when using this feature; no protection is applied on this input and damage to the target board may result if excessive voltage is applied. Also, do not attempt to power the target board through this connector while also applying power through the USB-Multilink BDM or the PWR connector; damage to the board may result.

Power may also be sourced to off-board circuitry through the J1 connector. The current supplied from the USB bus or the on-board regulator limits current available to external circuitry. Excessive current drain may damage the target board, the host PC USB hub, or the on-board regulator. The figure below details the VX_EN header connections.

Figure 5: VX_EN Option Header



CAUTION:

Do not exceed available current from USB-BDM or on-board regulator when sourcing power through connector J1 to external circuitry.

RESET SWITCH

The RESET switch applies an asynchronous RESET to the MCU. The RESET switch is connected directly to the RESET* input on the MCU. Pressing the RESET switch applies a low voltage level to the RESET* input. A pull-up bias resistor allows normal MCU operation. Shunt capacitance ensures an adequate input pulse width.

LOW VOLTAGE RESET

The MC9S08LG32 utilizes an internal Low Voltage Detect (LVD) circuit. The LVD holds the MCU in reset until applied voltage reaches an appropriate level. The LVD also protect against under-voltage conditions. Consult the MC9S08LG32 reference manual for details LVD operation.

TIMING

The DEMO9S08LG32 internal timing source is active from RESET by default. An external 32 kHz XTAL oscillator, configured for low-power operation, is also provided. Refer to the MC9S08LG32 Reference Manual for details on configuring the selected timing source.

COMMUNICATIONS

The DEMO9S08LG32 supports serial communications through the integrated USB-BDM and an on-board, low-voltage, RS-232 transceiver. The COM_SEL header selects the serial path applied. The 9-pin, D-Sub, connector at COM1 is not installed in default configurations.

USB SERIAL LINK

The integrated USB-BDM provides a serial link from the target MCU to the host PC through the host application. Refer to the P&E Multilink documentation for further details.

RS-232

An RS-232 translator provides RS-232 to TTL/CMOS logic level translation on the COM connector. The COM connector is a 9-pin Dsub, right-angle connector. A ferrite bead on shield ground provides conducted immunity protection. Communication signals TXD1 and RXD1 are routed from the transceiver to the MCU. Hardware flow control signals RTS and CTS are available on the logic side of the transceiver. These signals are routed to vias located near the transceiver. RTS has been biased properly to support 2-wire RS-232 communications.

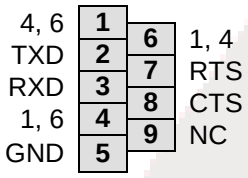
Figure 6: COM Connections

MCU Port	COM Signal	I/O PORT CONNECTOR
PTI1/TMRCLK/TX2	TXD	J1-5
PTI0/RX2	RXD	J1-7

COM Connector

A standard 9-pin Dsub connector provides external connections for the SCI0 port. The Dsub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. The figure below details the DB9 connector.

Figure 7: COM1 Connector



Female DB9 connector that interfaces to the MCU internal SCI0 serial port via the RS232 transceiver. Flow control is provided at test points on the board.

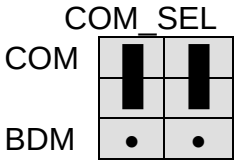
Pins 1, 4, and 6 are connected together.

NOTE: The COM1 connector is not installed in default configurations.

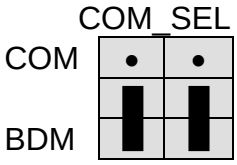
COM_SEL

The COM_SEL option header connects the MCU SCI port to either the SCI PHY or the USB-BDM connection. Figure 8 below shows the option jumper configuration for the COM_SEL option header.

Figure 8: COM_SEL Option



Enable UART COM to on-board SCI PHY and DB-9 connector
(NOTE: The DB9 connector is not installed in default configuration)



Enable UART COM to integrated USB-BDM connector

NOTE: The silkscreen marking for the COM_SEL header is incorrect on Rev A boards. The RXD position enables COM through the DB9 connector while the TXD position enables COM through the integrated USB-BDM.

LCD

The DEMO9S08LG32 provides a 4 x 40 custom LCD glass connected directly to the target MCU. Refer to the MC9S08LG32 Reference Manual for details on use and configuration.

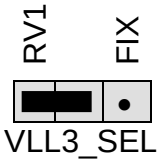
A row of option jumpers located below the LCD module allows each LCD signal to be disconnected from the associated LCD input. This allows multiplexed signal functionality to be used without affecting the LCD module.

The LCD Enable Option Header allows the user to disable any LCD signal to the LCD. This allows any signal to be used for a multiplexed function with out affecting the LCD. Figure 15, at the end of this document, shows the relation between target MCU signals and LCD glass pins through the JP1 option header. Installing a shunt at any position enables the LCD signal to the LCD. Removing a shunt at any position disconnects the LCD signal from the LCD.

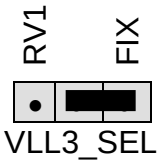
Contrast

LCD contrast control is controlled by the VLL3_SEL option header. This option header applies either fixed or variable LCD contrast. Variable contrast control requires the target board be powered from an external +12V power supply connected to VIN.

Figure 9: VLL3_SEL Option Header



Enable variable LCD Contrast Control



Set fixed contrast control

NOTE: Silkscreen on VLL3_SEL is incorrect. The RV1 selection actually connects to the CONTRAST POT and not the RV1 POT.

NOTE: Use of variable Contrast Control requires that +12V input be applied at VIN connector.

NOTE: VLL3_SEL must be set to FIX if target board is powered from integrated USB-BDM.

CAUTION

Voltage input at VIN greater than +12V may damage the target board.

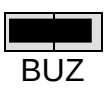
USER I/O

User I/O includes 2 potentiometer, 8 push button switches, and 8 green LEDs, and 1 piezo buzzer for user I/O. The User1, User2, and Buz option header blocks enable or disable each User I/O function individually.

Buzzer

The DEMO9S08LG32 target board provides an externally modulated piezo-buzzer for audible applications. A push-pull drive circuit allows the target MCU to easily drive the buzzer at a center frequency of 2300 Hz. Figure 10 below shows the USER enable position and associated signal for the buzzer.

Figure 10: BUZ Option Header



	ON	OFF
PTF3/TPM2CH5	Enabled	Disabled

Potentiometer

The DEMO9S08LG32 target board provides a 5K ohm potentiometer (POT) to simulate analog input. The POT is decoupled to minimize noise during adjustment. The POT is selectively assignable to ADC6 or ADC7 by the ADC option header.

The ADC option header also controls POT configuration. The POT may be configured as a variable pull-down resistance or may be connected to VDDA as a variable voltage input.

Figure 11 below shows the ADC option header selections.

Figure 11: ADC Option Header

ADC		Signal	ON	OFF
• •	PTH0	PTH0/KBI5/ADC6	Enabled	Disabled
• •	PTH1	PTH1/KBI6/ADC7	Enabled	Disabled
• •	VDDA	VDDA	Enabled	Disabled

CAUTION

While using pushbuttons KBI5 or KBI6 in end-user applications, the option jumper at PTH0 and, or, PTH1 should be removed. Pressing pushbutton KBI5 with option jumper installed at PTH0; or, pressing pushbutton KBI6 with option jumper installed at PTH1 will cause a target board POR.

User LED's

The DEMO9S08LG32 target board provides 8, green, LEDs for output indication. Each LED is configured for active-low operation. A series, current-limit resistor prevents excessive diode current. Figure 12 below shows the USER1 enable position and associated signal for each LED.

Figure 12: User1 Option Header

	USER2		Signal	ON	OFF
T1C0	• •	1	PTH5/TPM1CH0	Enabled	Disabled
T1C1	• •	2	PTH4/TPM1CH1	Enabled	Disabled
T2C0	• •	3	PTI5/TMP2CH0	Enabled	Disabled
T2C1	• •	4	PTI4/TPM2CH1	Enabled	Disabled
T2C2	• •	5	PTI3/TPM2CH2	Enabled	Disabled
T2C3	• •	6	PTF5/TMP2CH3	Enabled	Disabled
T2C4	• •	7	PTF4/TPM2CH4	Enabled	Disabled
T2C5	• •	8	PTF3/TPM2CH5	Enabled	Disabled

CAUTION

While using pushbuttons KBI5 or KBI6 in end-user applications, the option jumper at PTH0 and, or, PTH1 should be removed. Pressing pushbutton KBI5 with option jumper installed at PTH0; or, pressing pushbutton KBI6 with option jumper installed at PTH1 will cause a target board POR.

Pushbutton Switches

The DEMO9S08LG32 provides 8 push-button switches for user input. Each push-button switch is configured for active-low operation. No bias is applied to these push-button inputs. Use of target MCU internal pull-ups is required for proper operation. Figure 13 below shows the USER2 enable position and associated signal for each user switch.

Figure 13: User2 Option Header

USER1			Signal	ON	OFF
•	•	KBI1	PTH6/KBI1	Enabled	Disabled
•	•	KBI2	PTH7/KBI2	Enabled	Disabled
•	•	KBI3	PTH4/KBI3	Enabled	Disabled
•	•	KBI4	PTF0/KBI4	Enabled	Disabled
•	•	KBI5	PTH0/KBI5	Enabled	Disabled
•	•	KBI6	PTH1/KBI6	Enabled	Disabled
•	•	KBI7	PTH2/KBI7	Enabled	Disabled
•	•	KBI8	PTH3/KBI8	Enabled	Disabled

MCU I/O PORT

The MCU I/O PORT connector provides access to the MC9S08LG32 I/O signals. Figure 14 below show the pin-out for the MCU I/O connector.

Figure 14: MCU I/O PORT – J1

VDD	1	2	PTF2/SPSCK/TPM1CH1/IRQ/ADC14
VSS	3	4	PTC6/RESET*
PTI1/TMRCLK/TX2	5	6	PTC5/BKGD/MS
PTI0/RX2	7	8	PTA7/TCLK/ADC5/LCD28
PTH5/TX1/KBI4/TPM1CH0/ADC11	9	10	PTH2/KBI7/ADC8
PTH4/RX1/KBI3/TPM1CH1/ADC10	11	12	PTA6/KBI8/TPM2CH1/ADC4/LCD27
PTH7/KBI2/TPM2CH4	13	14	PTA5/KBI7/TPM2CH0/ADC3/LCD26
PTH6/TPM2CH5/KBI1/ADC15	15	16	PTA4/KBI6/RX2/ADC2/LCD25
PTI3/TPM2CH2/MOSI	17	18	PTA3/KBI5/TX2/ADC1/LCD24
PTI2/TPM2CH3/MISO	19	20	PTA0/LCD21
PTI4/TPM2CH1/SDA/SPSCK	21	22	PTH0/KBI5/ADC6
PTI5/TPM2CH0/SCL/SS*	23	24	PTH1/KBI6/ADC7
PTF6/XTAL	25	26	PTA1/SCL/LCD22
PTF7/EXTAL	27	28	PTA2/SDA/ADC0/LC23
PTD0/LCD0	29	30	PTH3/KBI8/ADC9
PTD1/LCD1	31	32	PTF3/SS*/KBI1/TPM2CH5
PTD2/LCD2	33	34	PTF5/MOSI/KBI3/TMP2CH3
PTD3/LCD3	35	36	PTF4/MISO/KBI2/TPM2CH4
PTD4/LCD4	37	38	PTF1_out/RX1/TPM1CH0/ADC13
PTD5/LCD5	39	40	PTF0/TX1/KBI4/TPM2CH2/ADC12
PTD6/LCD6	41	42	PTG0/LCD33
PTD7/LCD7	43	44	PTG1/LCD34
PTE0/LCD8	45	46	PTG2/LCD35
PTE1/LCD9	47	48	PTG3/LCD36
PTE2/LCD10	49	50	PTG4/LCD41
PTE3/LCD11	51	52	PTG5/LCD42
PTB3/LCD32	53	54	PTG6/LCD43
PTB2/LCD31	55	56	PTG7/LCD44
PTB6/LCD39	57	58	PTB7/LCD40
PTB4/LCD37	59	60	PTB5/LCD38
PTE4/LCD12	61	62	PTB1/LCD30
PTE5/LCD13	63	64	PTB0/LCD29
PTE6/LCD14	65	66	PTC0/LCD16
PTE7/LCD15	67	68	PTC1/LCD17
PTC4/LCD20	69	70	PTC2/LCD18
PTC3/LCD19	71	72	VCAP1
VDDA/VREFH	73	74	VCAP2
VSSA/VREFL	75	76	VLL1
VLL3	77	78	VLL2
VSS	79	80	VSS

LCD ENABLE OPTION HEADER

The LCD Enable Option Header allows the user to disable any LCD signal to the LCD. This allows any signal to be used for a multiplexed function with out affecting the LCD. Figure 15 below shows the relation between target MCU signals and LCD glass pins through the JP1 option header. Installing a shunt at any position enables the LCD signal to the LCD. Removing a shunt at any position disconnects the LCD signal from the LCD.

Figure 15: LCD Enable Option Header – JP1

MCU Pin #	MCU Signal	LCD Signal	JP1 Pos #	JP1 Pin		LCD Pin
14	PTB0/LCD29	LCD29	1	1	2	44
13	PTB1/LCD30	LCD30	2	3	4	43
12	PTB4/LCD37	LCD37	3	5	6	42
11	PTB5/LCD38	LCD38	4	7	8	41
10	PTB6/LCD39	LCD39	5	9	10	40
9	PTB7/LCD40	LCD40	6	11	12	39
8	PTB2/LCD31	LCD31	7	13	14	38
7	PTB3/LCD32	LCD32	8	15	16	37
16	PTD0/LCD0	LCD00	9	17	18	1
15	PTD1/LCD1	LCD01	10	19	20	2
6	PTD2/LCD2	LCD02	11	21	22	3
5	PTD3/LCD3	LCD03	12	23	24	4
4	PTD4/LCD4	LCD04	13	25	26	5
3	PTD5/LCD5	LCD05	14	27	28	6
2	PTD6/LCD6	LCD06	15	29	30	7
1	PTD7/LCD7	LCD07	16	31	32	8
80	PTE0/LCD8	LCD08	17	33	34	9
79	PTE1/LCD9	LCD09	18	35	36	10
78	PTE2/LCD10	LCD10	19	37	38	11
77	PTE3/LCD11	LCD11	20	39	40	12
76	PTE4/LCD12	LCD12	21	41	42	13
75	PTE5/LCD13	LCD13	22	43	44	14
74	PTG0/LCD33	LCD33	23	45	46	15
73	PTG1/LCD34	LCD34	24	47	48	16
72	PTG4/LCD41	LCD41	25	49	50	17
71	PTG5/LCD42	LCD42	26	51	52	18
70	PTG6/LCD43	LCD43	27	53	54	19
66	PTE6/LCD14	LCD14	28	55	56	20
65	PTE7/LCD15	LCD15	29	57	58	21
64	PTC0/LCD16	LCD16	30	59	60	22
63	PTC1/LCD17	LCD17	31	61	62	36
62	PTC2/LCD18	LCD18	32	63	64	35
61	PTC3/LCD19	LCD19	33	65	66	34
60	PTC4/LCD20	LCD20	34	67	68	33
59	PTA0/LCD21	LCD21	35	69	70	32
58	PTG2/LCD35	LCD35	36	71	72	31
57	PTG3/LCD36	LCD36	37	73	74	30
56	PTA1 /LCD22	LCD22	38	75	76	29
55	PTA2 /LC23	LCD23	39	77	78	28
54	PTA3 /LCD24	LCD24	40	79	80	27
53	PTA4 /LCD25	LCD25	41	81	82	26
52	PTA5 /LCD26	LCD26	42	83	84	25
51	PTA6 /LCD27	LCD27	43	85	86	24
50	PTA7 /LCD28	LCD28	44	87	88	23