CMD-12DP512

Development Board for the Freescale MC9S12DP512

Axiom Manufacturing • 2813 Industrial Lane • Garland, TX 75041
Email: Sales@axman.com Web: http://www.axman.com

CONTENTS

GETTING STARTED

The Axiom CMD-12DP512 single board computer is a fully assembled, fully functional development system for the Freescale MC9S12DP512 microcontroller. Provided with wall plug power supply, Serial cable, USB cable, and accessories. Support software for this development board is provided for Windows 95/98/NT/2000/XP operating systems. Additional compatible peripherals such as LCD display or keypad are available from Axiom as the HC-LCD and HC-KP respectfully. Lab kits are also available for different functions, contact Axiom or refer to the www.axman.com web site – educational pages for more details.

The 68HC12 support CD provided with the kit contains additional documentation, utility software, drawings, and software examples. The CD should be browsed to review all content. In each content folder on the CD will be a folder or directory named for the development board that has specific content. Published Utility software will also be found such as AxIDE.

Evaluation or application development may be performed by applying the embedded MON12 firmware monitor with AxIDE3 or with the AxIDE4 integrated compiler and debugger tools. The CMD-12DP512 board provides an integrated USB connection Background Debug Module (BDM) for application with AxIDE4. MON12 monitor application provides a serial port connection for evaluation and/or command line debug methods with AxIDE3. The AxIDE4 software provides a restore operation to reload the MON12 monitor if required.

The MON12 monitor is provided in the development board HCS12 internal flash memory by default when shipped. Monitor operation applies some HCS12 memory resources and requires a serial port connection for operation. See the MON12 User Manual for details on operation and resources applied. To apply AxIDE3 with the CMD-12DP512 MON12 firmware, the CML-12DP256 target board should be selected. The primary utility software referred to in this user manual will be AxIDE4 which provides the USB connection and C compiler tools.

Development board users should also be familiar with the hardware and software operation of the target M9S12DP512 MCU device, refer to the Freescale User Guides for the device and the CPU12 Reference Manual for software details. The development board purpose is to assist the user in quickly developing an application with a known working environment or to provide an evaluation platform for the target HCS12. Users should be familiar with memory mapping, memory types, and embedded software design for the fastest successful application development.

AxIDE4 application with the BDM connection allows all resources of the HCS12 to be applied by the user's application. Application development is Windows based with views of registers, memory, and source codes available. Building object code, loading the board, and managing the execution of the application are mouse click operations. Compiler tools are built with the GNU open source C compiler and assembler. Simple text based files control many features of the IDE and target. Easy editor launching allows modification of any source or control file for quick changes. Refer to the AxIDE4 software user manuals and help for details.

Follow the steps in this section to get started quickly and verify everything is working correctly.

Install the Software First

1. The CMD-12DP512 board MON12 monitor application may be evaluated without installing any software on the PC. Refer to the CMD-12DP512_MON12.pdf document. This user manual will provide details on options and development board features.

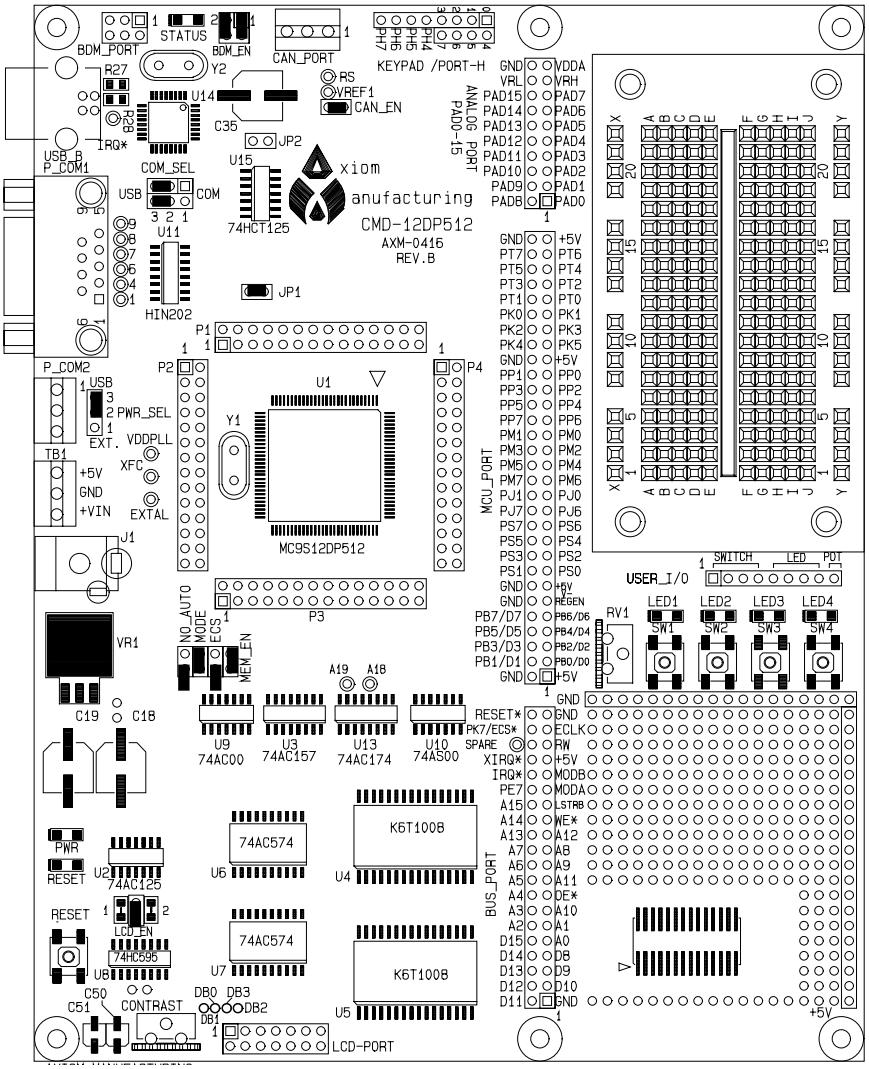
2. Refer to the AxIDE4 User Manual provided with the development kit to install the AxIDE4 software. The AxIDE4 software must be installed prior to connecting the CMD-12DP512 USB port to the host PC.

3. Browse the 68HC12 support CD for additional documents, application notes, MCU device user manuals and examples for the DP512 versions. These support documents will not be installed automatically and must be copied.

4. Set CMD-12DP512 options to default (review if USB power is not to power the board). Connect the USB cable to the host PC and the CMD board USB port.

CMD-12DP512 Default Option Settings

AxIDE4 USB Connection Settings



Default Options Summary

BDM_EN	IN (both)
CAN_EN	IN
COM_SEL	USB
JP1	IN
JP2	**OUT**
PWR_SEL	USB
LCD_EN	IN
NO_AUTO	OUT
MODE	IN
ECS	OUT
MEM_EN	IN

AxIDE4 OPERATION

The AxIDE4 software will apply the CMD-12DP512 USB port (BDM) for connection to the development board. Refer to the AxIDE4 User Manual for establishing a connection with the CMD-12DP512 board. The STATUS indicator near the USB port on the board provides an indication of connection with the software.

Connection to the development board is not required to edit and compile application software with AxIDE4. Connection is required to load or "Debug" the application on the board. User should note that the software Memory target type, register settings, and CMD-12DP512 board options must be set and reviewed together for proper operation when the application is loaded. Refer to the **Target Memory Option Table** to review these settings.

The CMD-12DP512 board may be configured to emulate HCS12 device internal flash memory in the external board Ram memory space. This feature allows the BDM (Background Debug Module) to load and control the execution of code being developed without the necessity of the internal flash memory being programmed.

Operation Notes for BDM use:

1) For BDM use the default HCS12 Mode is Single-Chip and the board MODE option installed. The BDM initialization of the HCS12 will set the correct operating Mode (Expanded Wide for external memory access) as required to properly load the board memory. The user application code should also perform the Expanded Wide configuration for external memory access even if the MODE is optioned for Expanded. See the MODE option for additional details.

2) While using the BDM, the user has full control over the memory map and hardware resources of the HCS12. No resources are required to be reserved and the user may apply the physical HCS12 interrupt vector table located at 0xFF80 - 0xFFFF. The internal HCS12 flash may be disabled for emulation of the flash memory space in the board external RAM memory. Refer to the HC12 MISC register for internal flash memory mapping options.

3) The BDM provides optional power and serial port connections, review limitations for these settings in the COM_SEL and PWR_SEL option sections.

TARGET MEMORY OPTION TABLE

This table provides a quick reference for software and hardware settings for the different target memory maps. Relocating the HCS12 internal EEprom, Internal Ram, and Register space is not provided here. Refer to the provided default target memory settings in the example projects for more details.

Target Memory Type	HCS12 Registers			CMD-12DP512 Memory Options		
	MODE	PEAR	MISC	MEM_EN	MODE	ECS
1) Single-Chip	Default	Default	Default	OFF	ON	OFF
2) Expanded with Flash	0xE0	0xC0	0x0F	ON	ON (BDM) OFF (Application)	OFF
3) Expanded without Flash	0xE0	0xC0	0x0C	ON	ON (BDM only)	OFF
4) Expanded w/ Paging	0xE2	0xC0	0x0F or 0x0C	ON	ON (BDM) OFF (Application)	ON

Notes:

1) The NO_AUTO option should be OFF when applying AXIDE4 or a BDM.

2) Single-chip mode provides all the HCS12 I/O ports including ports A and B for application. No external memory space (board memory) is available. Applications must apply flash, EEprom and internal ram. ECLK output is optioned in the PEAR register, refer to DP512 user manual. Flash is always capable of Program Paging. Flash Low Page appearing in the 0x4000 – 0x7FFF memory space is always PPAGE 0x3E.

3) Expand Mode allows external memory (board memory) access. HCS12 I/O ports A, B, and part of port E (ECLK, LSTRB, R/W) are applied for the memory bus. External RAM (board memory) is available.

4) In Expanded Mode the Flash may be optioned in the MISC register to be Off (not present) or High only (0xC000 – 0xFFFF) with Page space (0x8000 – 0xBFFF per PPAGE register setting). The Flash Low Page is normally disabled to allow access to external RAM (board memory). If the Flash is optioned Off, the external RAM (Board memory) will be present in the Flash memory space if the settings in the table above are provided. The Flash may only be OFF during BDM application, user applications must reside in Flash memory for operation without the BDM.

5) Expanded with Paging operation will apply Port K as an external memory address port, Port K will not be available for I/O operations. The Flash will always occupy Program Pages (PPAGE register) 0x20 to 0x3F when enabled. External Ram (Board memory) may occupy Program Pages not occupied by the Flash. External RAM only provides 16 PPAGES (0x10 – 0x1F for instance) or 256K bytes. External Ram appearing in memory space 0x4000 – 0x7FFF will also be the PPAGE 0x1E page when Expanded Paging with Flash is enabled or any PPAGE 0x--E page with Flash disabled.

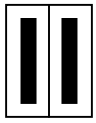
OPTIONS and JUMPERS

Option Summary – REV A.

BDM_EN	Enable the USB port BDM for AxIDE4 to control the HCS12.
MEM_EN	Enable the External RAM (Board memory).
MODE	Select HCS12 operating Mode from Reset.
ECS	Enable External Memory Paging in Expanded Mode (MODE EMK bit must be set also).
NO_AUTO	Disable MON12 AUTOSTART operation. Default = Open.
PWR_SEL	Select CMD-12DP512 power source: PWR jack and +5V regulator, USB port, or external. See PWR_SEL option for details.
COM_SEL	Select HCS12 SCI0 serial path: P_COM1, USB, or external. See the COM_SEL option for details.
JP1	Enable the P_COM2 port receive on HCS12 SCI1 / I/O port PS2. See P_COM2 for details.
CAN_EN	Enable the CAN port receive signal on HCS12 I/O port PM0. See CAN Port for details.
LCD_EN	Enable the LCD Port to be selected by SPI0 SS0* signal on HCS12 I/O Port PS7. See LCD Port for details.
JP2	Not Installed, see JP2 option for details.
CUT_AWAY 1,2, 6	Hard Options, See LCD for 1 and 2, see CAN Port for 6.

BDM_EN Option

The two BDM_EN option jumpers are open by default. These option should be Installed when applying AxIDE4 and the CMD-12DP512 USB port. Jumpers must be open or idle at all other times.



BDM_ON

MEM_EN Option

The MEM_EN option jumper is installed by default and enables the External RAM memory (Board Memory) on the Expanded HCS12 address and data bus. Removing the MEM_EN option jumper will remove the Board Memory from the Expanded memory bus. MEM_EN should be open when applying Single-chip mode operation and HCS12 Ports A and B, these are the Expanded memory bus ports.

MODE Option

The MODE option jumper is installed by default for BDM application. The option allows the selection at Reset of Single-chip Mode (installed) or Expanded Wide Mode (open) operation for user applications of the HCS12. Single-chip Mode provides all I/O ports and no external memory. Expanded Wide Mode provides the external memory bus and applies Ports A, B, part of E, and optionally K for memory bus use. Port K application is determined by the Mode register EMK bit setting at Reset initialization time.

ECS Option

The ECS option installed enables the upper address signals (A14 – A19) from Port K of the HCS12 to drive the upper address lines of the external Ram on the board. This provides external memory Paging capability to the memory bus. The HCS12 MODE register must have the EMK bit set to support this operation also. With the ECS option open or idle, only the linear 64K byte address map is available on the external address / data bus.

NO_AUTO Option

The NOAUTO option jumper should be open or off normally. The option applies a ground potential to the Port E0 / XIRQ* interrupt line. Option is applied for MON12 operation, refer to the CMD-12DP512 MON12 user manual for details.

INDICATORS

Indication is provided for power supply status, HCS12 Reset status, and User application.net status. The indications may be applied to determine proper operation of the development board or the Users application.

Indicator Summary

INDICATOR	COLOR	OPERATION	DEFAULT CONDITION
PWR	Green	+5V Logic voltage present	ON
RESET	RED	HCS12 is in RESET state	OFF
STATUS	Green	USB BDM status indicator	ON or flashing with USB connection
LED1 - 4	Green	ON with logic 1 or +5V applied to respective input on USER I/O connector.	Application specific Refer to USER I/O connector

SWITCHES

Push switches RESET and SW1 – 4 are provided for manual Reset of the HCS12 and for User Application respectfully. All switches provide an active low or 0 volt output when depressed and no connection when released.

Switch Summary

SWITCH	OPERATION
RESET	Manual Reset of HCS12, forces Reset signal low. Reset Indicator will be ON while switch is depressed.
LED1 - 4	User Application switches. Refer to USER I/O connector for details.

POWER Supply and Reset

DC voltage to power the board may be applied by the USB port (default), J1 Power Jack, or externally from the TB1 term block. The PWR_SEL option determines the source. The +VIN signal from TB1 or the J1 power jack is the input supply voltage to the board +5V voltage regulator VR1. +VIN voltage range is +8VDC to +20VDC. When the J1 Power jack is applied for input, the TB1 +VIN connection may be applied to source other circuits within the limits of the wall-plug or power source current capacity or 2 Amps maximum in any case.

The VR1 +5V DC Regulator will provide 300ma total current with the board components applying up to 100ma of this total. With +9VDC as the typical applied input voltage the user may apply up to 200ma of the +5V safely. VR1 current capacity will be reduced due to heat build up if input voltage is higher. Application should limit VR1 power to 3 watts.

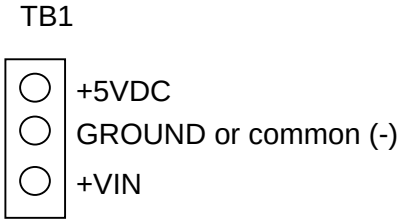
J1 Power Jack

The J1 power jack accepts a standard 2.0 ~ 2.1mm center barrel plug connector (positive voltage center) to provide the +VIN supply.

+Volts, 2mm center

TB1 Power Term Block

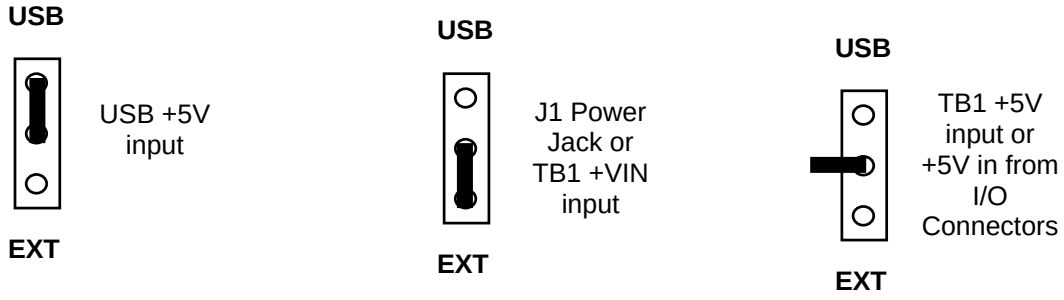
TB1 provides access to the +VIN, GND (power ground), and +5V logic power supplies. +VIN input power should only be applied by J1 or TB1, not both or a supply conflict may occur. The +5V logic supply may be accessed at TB1 for user circuit application with in the current limits of VR1. TB1 +5V connection may also source the +5V logic supply when the POWER option is open or idle. The +5V source must be regulated and with in the 4.9V to 5.1V range.



PWR_SEL Option

The PWR_SEL option enables the enables the +5VDC from the CMD-12DP512 on board VR1 voltage regulator or USB BDM +5V to the board circuits. If the user requires applying external +5VDC by TB1 connection to the CMD-12DP512 board, the PWR_SEL option must be opened or idled. Applying external +5VDC is not recommended and may damage the CMD-12DP512 board if not properly regulated. User may apply a separate +5VDC for user circuit application and apply the GND / Common connection instead. If a separate +5V supply is applied, caution should be applied not to connect the on board +5V to the external +5V supply.

The USB power option position is limited to 200ma total. The USB power option should not be applied if external circuits are applied on the CMD-12DP512 board.



RESET

The HCS12 Reset has several sources and is indicated active by the RESET indicator. The Reset indicator will be ON for the duration of Reset signal being active. If the Reset indicator is ON constantly there is an issue that is preventing the HCS12 from executing or causing the Reset signal to be applied active (logic low or 0 volts). When RESET is active no HCS12 operation is possible.

On-board Reset is provided by the USB BDM port (BDM_ON options are installed), BDM Port (development cable connected), RESET switch (depressed), LV1 voltage detector (+5V too low condition), HCS12 (oscillator or COP watchdog), and the BUS Port (Reset signal). User should review the possible cause and clear the issue to operate the CMD-12DP512 board.

COMMUNICATION Ports

The CMD-12DP512 provides 4 communication ports with interfaces. The ports provided are the P_COM1 (SCI0) serial port, P_COM2 (SCI1) serial port, CAN (MSCAN0) serial port, and the USB port for BDM application.

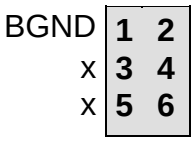
USB_B Port (BDM)

The USB_B port is dedicated to interface with a host PC operating the AxIDE4 software. When this port is applied the BDM_ON options should be installed to allow interface to the HCS12. This port and the BDM Port should not be applied at the same time.

BDM_PORT

The BDM Port is a standard development cable connection provided for other types of BDM / debug cable interfaces if wanted. The host PC must be operating the necessary software to control the cable type connected. When this port is applied the BDM_ON options should be Open or idle to allow interface to the HCS12 by this port. This port and the USB Port should not be applied at the same time.

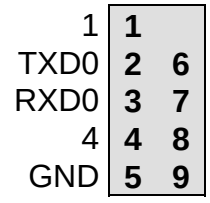
The BDM port is a 6 pin header compatible with the Freescale Background Debug Mode (BDM) Pod.



See the HC12 Technical Reference Manual for complete documentation of the BDM.

The on-board USB BDM must be disabled by BDM_ON option OPEN to apply this port.

P_COM1



Female DB9 type connector that interfaces to the HCS12 internal SCI0 serial port via the U11 RS232 transceiver. It uses a simple 2 wire asynchronous serial interface and is translated to RS232 signaling levels.
1,4,6 connected and 7,8 connected

JP1 will isolate the SCI0 pins from the transceiver.

The 1,4,6,7,8, and 9 pins provide RS232 flow control and status. These are connected on the on the bottom of the development board to provide NULL status to the host. User may isolate pins and provide flow control or status connection to the host by applying HCS12 I/O signals and **RS232 level conversion.**

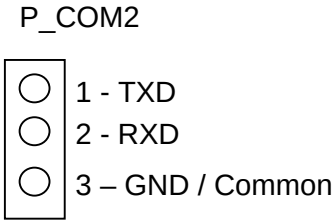
COM_SEL Option

COM_SEL provides selection of the P-COM1 RS232 port or the USB BDM virtual COM port for the HCS12 SCI0 serial port interface. The option may be open to allow user connection of SCI0 or I/O pins to another applied device. SCI0 is provided from the HCS12 Port S0 and S1 pins.

P_COM1 Port selection USB Port selection

P_COM2

P_COM2 is a 3 pin Terminal Block that provides the HCS12 SCI1 serial port translated to RS232 signal levels. A solder cup DB9 style connector may be installed with wires and connector to apply this channel. JP2 option will isolate the SCI RXD pin from the transceiver.



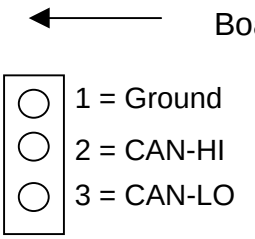
JP1 – SCI1 Select Option

JP1 provides selection of the P-COM2 RS232 port for RS232 receive path to SCI1. JP2 installed connects the SCI1 RXD port (Port S3) to the P-COM2 RS232 transceiver. HCS12 Ports S2 and S3 provide the SCI1 signals.

CAN PORT

This port provides a CAN Bus interface associated with HCS12 CAN channel 0. The port has a CAN Transceiver (Philips PCA82C250) capable of up to 1M Baud data rate. The user may isolate the HCS12 CAN channel 0 RXD signal (port PM0) from the transceiver by CAN_EN option jumper. Cut-Away option 6 allows further control of the transceiver operation.

CAN Port



CAN_EN Option

CAN_EN installed provides the CAN RX signal to the HCS12 CAN-0 RX input pin (port PM0). Open the enable option to apply the HCS12 Port PM0 pin for other applications.

Cut-Away #6, CAN BUS TRANSMIT ENABLE

The CAN port transceiver transmit driver is enabled by default for maximum drive and minimum slew rate by default. The drive and slew rate may be adjusted by cutting CUT-AWAY #6 and adding an 0805 size surface mount resistor, see the PCA82C250 data sheet for more information.

CAN Bus transceiver transmit enable control can be applied to the port by the RS tie pad. The user should select an available HCS12 I/O port to perform the transmit enable function and connect it from the MCU_PORT pin to RS pad as required. **The CUT_AWAY #6 must be open to apply transmit enable control.** The transmit enable signal to the CAN transceivers is active logic low.

CUT-AWAY options allow the user to disconnect dedicated HCS12 I/O port resources from development board peripherals. The CUT-AWAY options also allow for establishing the connection again by installing surface mount 0805 size 0 ohm resistors or mod wire with the use of a soldering iron. Normal operation of the development board generally does not require any manipulation of the CUT_AWAY options.**CAN BUS TERMINATION**

The CAN port provides RC1 as 120 Ohms to terminate the CAN bus. User may change this 0805 size SMT resistor if required for application.

JP2 Option

JP2 is provided for possible future USB BDM firmware updates. JP2 should remain open for normal operation of the USB port.

USER Accessory Ports

The LCD Port, Keypad Port, and USER I/O connector provide access to the user application accessory ports or on-board user indicators and switches.

LCD_PORT

The LCD_PORT interface is connected to the HCS12 SPI-0 port and applies a serial shift register to convert the data to parallel interface for LCD input. This is required due to the fast timing characteristics of the HCS12 data bus and the slow timing of the standard LCD Modules. Example LCD Port driver software is provided on the support CD to demonstrate typical LCD module operation using this technique.

The interface supports all OPTREX™ DMC series and similar displays with up to 80 characters in 4 bit bus mode and provides the most common pin out for a dual row rear mounted display connector. The LCD module VEE or contrast potential is 0 Volts on this board. The LCD module type should be TN (Standard Twist) style and Reflective to support this VEE potential. The Axiom HC-LCD is also compatible. The LCD Module is configured in a Write only mode, it is not possible to read current cursor position or the busy status back from the module.

LCD_PORT Connector

+5V	2	1	GND	SPI data bit definitions to LCD Port:
RS	4	3	CONTRAST	D0 - D3 = DB4 - 7, LCD data
EN	6	5	R/W-GND	D4 - D5 = Spare pins S1 and S2, not connected
DB1	8	7	DB0	D6 = RS, 0 = LCD Command, 1 = LCD Data
DB3	10	9	DB2	D7 = EN, 1 = LCD enable.
DB5	12	11	DB4	DB0 –DB3 are not applied and have 10K pull-down
DB7	14	13	DB6	resistance.

NOTES:
1) The LCD write requires 3 SPI transfers. Transfer 1 provides data 0 - 3 and RS (register select) value. Transfer 2 provides the same data with the EN (D7) bit set. Transfer 3 provides same data with the EN bit clear. See the KLCD examples for operation.
2) CUT-AWAY 1 and 2 provide a means to isolate the LCD Port from the HCS12 SPI channel.

CUT-AWAY options allow the user to disconnect dedicated HCS12 I/O port resources from development board peripherals. The CUT-AWAY options also allow for establishing the connection again by installing surface mount 0805 size 0 ohm resistors or mod wire with the use of a soldering iron. Normal operation of the development board generally does not require any manipulation of the CUT_AWAY options.

#1 Cut-Away: HCS12 Port S5/MOSI signal to the LCD_PORT shift register.
#2 Cut-Away: HCS12 Port S7/SS0 signal to the LCD_PORT shift register.

CONTRAST

The contrast adjust potentiometer will provide a -5V to +5V potential for LCD contrast.

LCD_EN Option

The LCD_EN option IN provides the SPI-0 SS* (port PS7) select signal to the on-board LCD port. The select signal enables the LCD Port operation. With LCD_EN Open or Idle the LCD port will be disabled and SPI-0 SS* signal (PS7) may be applied to other applications.

KEYPAD / PORT H

The KEYPAD / PORT H connector provides interface for the HCS12 port H or for applying a keypad such as the Axiom Mfg. HC-KP. When applied as a KEYPAD connector, the interface is for a passive 4 x 4 matrix (16 key) keypad device. the port is optioned for a 1x8 keypad connector or a 2x4 keypad connector.

PH0	**1**	**1**	PH4
PH1	**2**	**2**	PH5
PH2	**3**	**3**	PH6
PH3	**4**	**4**	PH7
PH4	**5**		
PH5	**6**		
PH6	**7**		
PH7	**8**		

This interface is implemented as a software key scan. Pins PH0-3 are used as column drivers which are active high outputs. Pins PH4-7 are used for row input and will read high when their row is high.

See the **Keypad** example programs for applying this connector.

USER I/O Connector

The USER I/O connector provides access to the user LED1 – 4 indicators, SW1 – 4 push switches, and RV1 potentiometer. User LED inputs are 0 to 5V compliant and the respective indicator will be ON with logic high or +5V level applied. The SW1 – 4 push switches provide an active logic low or 0 volts output when depressed. For HCS12 input port application the detection of the switch active or inactive level may need de-bounce applied in software to validate the condition. RV1 provides a 0 to 5V analog output. Total RV1 resistance is 5K ohms. The RV1 output level may be input to the HCS12 analog input(s) or to user applications in the bread board or prototyping areas.

USER I/O

1	SW1 output
2	SW2 output
3	SW3 output
4	SW4 output
5	LED1 input
6	LED2 input
7	LED3 input
8	LED4 input
9	RV1 output

BREADBOARD and Prototype Area

The breadboard provides an easy work space to quickly install leaded parts and connect them to the HCS12 I/O or board power supply. The side rail component holes are bussed to allow power supply connections or other multi tap signal applications. The I/O port connectors provide a standard hole size to apply 22 – 24 gauge solid core wire between the connectors and breadboard.

The Prototype area allows for installation of components, connectors, or adapters by wire wrap or soldering methods. The grid is .1 inch and suitable for DIP package IC's or .025 square or round pins to be applied. The surface mount portion provides SOIC type or .50 lead pitch IC's to be applied. Each SMT pad has a through hole type pad provided for easy connection.

I/O Port connectors

The port connectors are organized by HCS12 I/O port or operation. Caution should be applied so that on-board connections to not conflict with user application. The HCS12 ports A, B, part of E, and optionally K will be memory bus ports when the HCS12 operating mode is Expanded. I/O connection is not possible to memory bus ports, either single-chip mode must be applied or a proper BUS port connection to memory bus access devices.

MCU_PORT

GND	**60**	**59**	+5V
PT7	**58**	**57**	PT6
PT5	**56**	**55**	PT4
PT3	**54**	**53**	PT2
PT1	**52**	**51**	PT0
** PK0	**50**	**49**	PK1 **
** PK2	**48**	**47**	PK3 **
** PK4	**46**	**45**	PK5 **
GND	**44**	**43**	+5V
PP1	**42**	**41**	PP0
PP3	**40**	**39**	PP2
PP5	**38**	**37**	PP4
PP7	**36**	**35**	PP6
** PM1	**34**	**33**	PM0 **
PM3	**32**	**31**	PM2
PM5	**30**	**29**	PM4
PM7	**28**	**27**	PM6
PJ1	**26**	**25**	PJ0
PJ7	**24**	**23**	PJ6
** PS7	**22**	**21**	PS6 **
** PS5	**20**	**19**	PS4 **
** PS3	**18**	**17**	PS2 **
** PS1	**16**	**15**	PS0 **
GND	**14**	**13**	+5V
GND	**12**	**11**	VREGEN
** PB7/D7	**10**	**9**	PB6/D6 **
** PB5/D5	**8**	**7**	PB4/D4 **
** PB3/D3	**6**	**5**	PB2/D2 **
** PB1/D1	**4**	**3**	PB0/D0 **
GND	**2**	**1**	+5V

The **MCU_PORT** provides access to the peripheral features and I/O lines of the HCS12.

** Note signals with alternate connections on the development board:

PB0 – 7 [D0 - 7] provide address / data on the expanded HCS12.

PK0 – 5 [XA14 - XA19] provide high order paged address lines on the expanded HCS12 with ECS enabled.

PM0 – 1 [CAN RXD0, TXD0] CAN channel 0 to CAN Port transceiver.

PS0 – 1 [COM Port RXD0, TXD0]

PS2 – 3 [JP3 Port RXD1, TXD2]

PS4 – 7 [SPI Port] provides LCD_PORT serial interface.

ANALOG PORT

GND	20	19	VDDA
VRL	18	17	VRH
PAD15/AN15	16	15	PAD7/AN7
PAD14/AN14	14	13	PAD6/AN6
PAD13/AN13	12	11	PAD5/AN5
PAD12/AN12	10	9	PAD4/AN4
PAD11/AN11	8	7	PAD3/AN3
PAD10/AN10	6	5	PAD2/AN2
PAD9/AN9	4	3	PAD1/AN1
PAD8/AN8	2	1	PAD0/AN0

The **ANALOG** port provides access to the Port AD0 and Port AD1 Analog-to-Digital input lines.

PAD0 – PAD15 HC12 Port AD0-15 is an input port or AN0 - AN15 A/D Converter inputs.

VRH / VRL HC12 A/D Converter Reference Pins. See HCS12 A/D User guide. To provide an external reference voltage, R3 and R4 need to be removed to apply external VRH or VRL respectfully. See schematic.

BUS_PORT

RESET*	40	39	GND
PK7/ECS	38	37	PE4/ECLK
SPARE	36	35	PE2/RW
PE0/XIRQ*	34	33	+5V
PE1/IRQ*	32	31	PE6/MODB
PE7	30	29	PE5/MODA
A15	28	27	PE3/LSTRB*
A14	26	25	WE*
A13	24	23	A12
A7	22	21	A8
A6	20	19	A9
A5	18	17	A11
A4	16	15	OE*
A3	14	13	A10
A2	12	11	A1
D15/PA7	10	9	A0
D14/PA6	8	7	PA0/D8
D13/PA5	6	5	PA1/D9
D12/PA4	4	3	PA2/D10
D11/PA3	2	1	GND

The **BUS_PORT** supports off-board memory devices while the HCS12 is in expanded mode.

PA0/D8 - PA7/D15 High Byte Data Bus in Wide Expanded Mode. Port A in Single Chip Mode.

A0 – A15 Latched Memory Addresses 0 to 15.

OE* Memory Output Enable signal, Active Low. Valid with ECLK and R/W high.

WE* Memory Write Enable signal, Active Low. Valid with ECLK high and R/W low.

RESET* HCS12 active low RESET signal.

P1 - P4 HCS12 Header Ring

P1 - P4 provide a header ring for all I/O of the HCS12 device. These connectors are not installed. User should refer to the CML12S board schematic diagram for connector pin connections. All HCS12 I/O is available from the other I/O Ports on the board.

TEST POINTS

The following test points are provided on the development board:

EXTAL : HCS12 oscillator or external clock input pin.

XTAL : HCS12 oscillator output pin.

XFC : HCS12 PLL reference voltage and filter.

VDDPLL : HCS12 PLL voltage source test point.

TROUBLESHOOTING

The CMD-12DP512 board is fully tested and operational before shipping. If it fails to function properly, inspect the board for obvious physical damage first. Review the GETTING STARTED section of this manual and verify the option settings and connections. See the **Tips and Suggestions** sections following for more information.

1. USB connection suspect: Follow these steps to verify USB operation –

    a) Disconnect the CMD-12DP512 board USB connector, power connection, and close the AxIDE4 software.

    b) Connect the CMD-12DP512 USB port to the host PC and verify the USB connection is recognized by the PC. Board STATUS indicator should be ON.

    c) Connect power to the CMD-12DP512 board and verify PWR Indicator is ON.

    d) Launch the AxIDE4 software and select the Tester window. Verify connection by performing Tester commands.

2. NO PWR indicator: Verify the power source and POWER option is installed. +8 volts DC or higher voltage may be measured between the GND and +VIN connections on the TB1 power connector with the standard power supply provided and plugged into the J1 connector.

3. If no voltage is found, verify the wall plug connections to AC wall plug outlet and the power connector. If applying a power strip make sure it is turned ON.

4. Verify the logic power source. Measure +5 volts between the GND and +5V connections on the TB1 power connector. If the +VIN supply is good and this supply is not +5V, immediately disconnect power from the board. Contact support@axman.com by email for instructions and provide board name and problem.

5. Disconnect all external connections from the CMD-12DP512 board except for USB to the PC and the wall plug.

6. Make sure that the RESET Indicator is not on all the time.

7. Contact support@axman.com by email for further assistance. Provide board name and describe problem.

Tips and Suggestions

Following are a number of tips, suggestions, and answers to common questions that will solve many problems. Download the latest software from the www.axman.com Support – software section of our web pages.

- Verify option settings, operating mode, and memory target.
- Review I/O connections with on-board connections and HCS12 operating mode restrictions on I/O ports.
- Make sure the correct power is supplied to the board. Only use a 9 volt, 200mA minimum adapter (provided) or power supply. If applying a power strip, make sure it is turned on.
- Make sure application code is in an address space that actually exists in memory (memory present at the address). The MODE, MEM_EN and ECS options change the memory map.
- When running code as stand-alone application, initialize ALL peripherals used by the HCS12 including the Stack, Serial Ports, and MODE / PEAR registers, and oscillator. The USB BDM may perform some initialization in a script file, review and test with these settings disabled. If Paging external memory make sure the EMK bit is being set in the MODE register.
- Disable the COP watchdog timer (clear COPCTL) or service the COP timer in the main loop of the application code. The HCS12 will enable the COP by default and it will reset the HCS12 every few 100ms. The COP timer does not run when the USB BDM or other BDM is controlling the HCS12.

TABLE 1: LCD Command and Character Codes

Command codes are used for LCD setup and control of character and cursor position. All data is sent to the LCD panel via the SPI interface. Port PS7/SS* controls the select line. See the example keylcd software for operation.

LCD Character Codes

$20	Space	$2D	-	$3A	:	$47	G	$54	T	$61	A	$6E	n	$7B	{
$21	!	$2E	.	$3B	;	$48	H	$55	U	$62	B	$6F	o	$7C	|
$22	“	$2F	/	$3C	{	$49	I	$56	V	$63	C	$70	p	$7D	}
$23	#	$30	0	$3D	=	$4A	J	$57	W	$64	D	$71	q	$7E	>
$24	$	$31	1	$3E	}	$4B	K	$58	X	$65	E	$72	r	$7F	<
$25	%	$32	2	$3F	?	$4C	L	$59	Y	$66	F	$73	s		
$26	&	$33	3	$40	Time	$4D	M	$5A	Z	$67	G	$74	t		
$27	‘	$34	4	$41	A	$4E	N	$5B	[	$68	H	$75	u		
$28	(	$35	5	$42	B	$4F	O	$5C	Yen	$69	I	$76	v		
$29	)	$36	6	$43	C	$50	P	$5D	]	$6A	J	$77	w		
$2A	*	$37	7	$44	D	$51	Q	$5E	^	$6B	K	$78	x		
$2B	+	$38	8	$45	E	$52	R	$5F	_	$6C	L	$79	y		
$2C	,	$39	9	$46	F	$53	S	$60	`	$6D	M	$7A	z		

LCD Command Codes

Note the delay required after commands are issued to the display module.

Command	Code	Delay
Clear Display, Cursor to Home	**$01**	1.65ms
Cursor to Home	**$02**	1.65ms
Entry Mode:		
Cursor Decrement, Shift off	**$04**	40us
Cursor Decrement, Shift on	**$05**	40us
Cursor Increment, Shift off	**$06**	40us
Cursor Increment, Shift on	**$07**	40us
Display Control:		
Display, Cursor, and Cursor Blink off	**$08**	40us
Display on, Cursor and Cursor Blink off	**$0C**	40us
Display and Cursor on, Cursor Blink off	**$0E**	40us
Display, Cursor, and Cursor Blink on	**$0F**	40us
Cursor / Display Shift: (nondestructive move)		
Cursor shift left	**$10**	40us
Cursor shift right	**$14**	40us
Display shift left	**$18**	40us
Display shift right	**$1C**	40us
Display Function (default 2x40 size)	**$3C**	40us
Character Generator Ram Address set	**$40-$7F**	40us
Display Ram Address and set cursor location	**$80- $FF**	40us