Freescale Semiconductor
User Guide

SLKS12UG
Rev. 0.4, 11/2010

APPLICATION MODULE STUDENT LEARNING KIT FEATURING FREESCALE HCS12

For use with the following part numbers:

Freescale Part Number:
APS12C128SLK (w/ integrated USB-BDM)
APS12DT256SLK (w/ integrated USB-BDM)
APS12XDT512SLK (w/ integrated USB-BDM)

Board Markings:
APS12

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Revision History

Date	Rev	Comments
November 4, 2010	0	Initial Release
October 2008	0.1	Updated document contents. Mark BDM header as not populated, and removed reference to power supply
December 18, 2008	0.2	Modified Board Name on title page. Updated Board drawings
December 7, 2009	0.3	Added section for BDM_EN option header
November 4, 2010	0.4	Updated contents, corrected errors, updated formatting

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the application module:

   a) This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development module uses option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed - jumper is installed such that 2 pins are connected together

Jumper off, out, or idle - jumper is installed on 1 pin only. It is recommended that jumpers be idled by installing on 1 pin so they will not be lost.

Project Board – Optional component which provides a common expansion and prototyping platform to enhance the learning feature set of multiple microcontroller application modules.

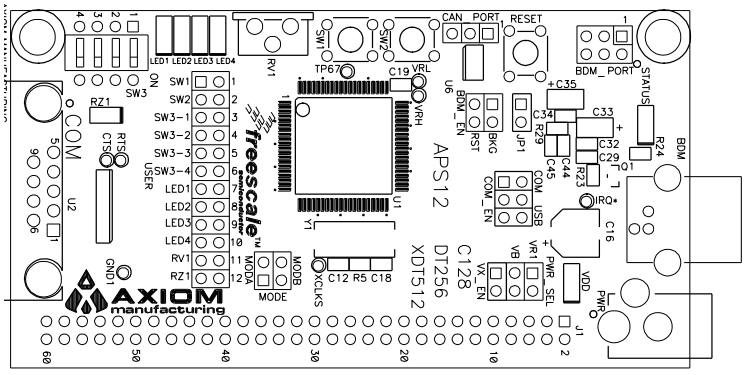
Application Module – A microcontroller development board featuring a Freescale Microcontroller.

FEATURES

- MC9S12 C128/DT256/XDT512 MCU, 80 LQFP
  - 128/256/512 KB Flash EEPROM
  - 4KB EEPROM
  - 12 KB RAM
  - SAE J1850 Byte Data Link Controller
  - 8-ch, 10-bit, ATD w/ external trigger
  - 8-bit Enhanced Capture Timer with IC, OC, and Pulse Accumulate capabilities
  - 7-ch, 8-bit PWM
  - 9 KBI inputs
  - 56 GPIO
  - 3 CAN Channels
  - CAN 2.0 A/B PHY w/ 3-pos header
  - 2 SCI & 2 SPI Channels
  - 1 IIC Channel
- RS-232 transceiver w/ DB9 connector
- 4 MHz Clock Oscillator
- Low Voltage Reset Supervisor
- Power Input Selection Header
- On-board 5V regulator
- Optional power Input/Output from ConnectorJ1

User Components Provided
  - 1 DIP Switch, 4-pos
  - 3 Push Button Switches: 2 User, RESET
  - 5 LED Indicators: 4 User, +5V
- Jumpers
  - USER_EN
  - PWR_SEL
  - COM_EN
- Connectors
  - 60-pos pin-header providing access to MCU IO signals
  - 2.0mm barrel connector power input
  - 6-pin BDM interface connector
  - 3-pos CAN interface connector
  - DB9 connector
- Supplied with DB9 Serial Cable, Power Supply, Documentation (CD), and Manual

Specifications:
Module Size 3.8” x 2.0”
Power Input: +9V typical, +6V to +18



ABOUT THE APPLICATION MODULE

This application module is an educational development module supporting multiple Freescale HCS12 family microcontrollers (MCU). There are three chipsets available with this application module, the S12C128, the S12DT256 and the S12XDT512.

Determining which microcontroller is on the application module

On the top of each application module you will see a listing of the three available microcontrollers C128, DT256, and XDT512 as show in Figure 1. Microcontroller Option Markings. The marked selection corresponds to the installed MCU.

Figure 1. Microcontroller Option Markings

Application module student learning kits include components for out-of-box operation. An integrated USB background debug (BDM) interface is provided for easy development tool use. The 60-pin connector allows the application module to be connected to an expanded evaluation environment such as the Microcontroller Project Board Student Learning Kit (PBMCUSLK) or user's custom PCB.

REFERENCES

The latest product information, updates and reference documents can be found at www.freescale.com and/or www.axman.com

SLKS12UG.pdf	APS12SLK User Guide (this document)
CSMB12_SCH_A.pdf	Application Module Schematic
S12QSG.pdf	Quick Start Guide for stand alone module operation
UVP_S12_DEMO.zip	CodeWarrior Project to support APS12PG

For the microcontroller specific information such as memory mapping, registers, programming, datasheet and all other device information visit www.freescale.com and search for MC9S12C128, MC9S12DT256, or MC9S12XDT512.

NOTE

For current product information, reference materials and updates visit
www.freescale.com\universityprograms

GETTING STARTED

Please refer to the Quick Start Users Guide to quickly setup and get started using the stand-alone application module or with the Freescale Project Board/Application Module.

NOTE

Please refer to the Quick Start Guide for illustrated guide to connecting the USB, and getting started with CodeWarrior.

DEVELOPMENT SUPPORT

SOFTWARE DEVELOPMENT

Software development requires the use of an HCS12 assembler or compiler and a host PC operating a debug interface. Supplied with this board is the CodeWarrior Development Studio for HCS12. CodeWarrior is a fully integrated development environment offering code editing, compilation, programming and debugging of Freescale Semiconductors. Users can program in both assembly and C/C++ with CodeWarrior.

MEMORY MAP

This application module is designed to support multiple HCS12 family microcontrollers specifically the S12C, S12DT, and S12XDT family of MCU's. This section shows the default memory map for each MCU immediately out of reset. Refer to the specific MCU Reference Manual for further details.

Table 1: C128 Memory Map

0x0000 – 0x03FF	Registers	1K bytes	Map to any 2K block in the first 2K boundary
0x0400 – 0x2FFF	EEPROM	16K bytes	Fixed Flash EEPROM
0x3000 – 0x3FFF	RAM	4K bytes	Map to any 4K boundary
0x4000 – 0x7FFF	Fixed FLASH	16K bytes	
0x8000 – 0xBFFF	Paged FLASH	128K bytes	8 – 16K pages
0xC000 –	Fixed Flash	16K	

0xFEFF		bytes	
0xFF00 – 0xFFFF	Vectors	256 bytes	BDM if active

Table 2: DT256 Memory Map

0x0000 – 0x03FF	Registers	1K bytes	Map to any 2K block in the first 32K
0x0400 – 0x0FFF	EEPROM	4K bytes	Map to any 4K block. Bottom 1K used by Registers out of reset
0x1000 – 0x3FFF	RAM	12K bytes	Map to any 16K block Align top or bottom
0x4000 – 0x7FFF	Fixed FLASH	16K bytes	Dependant on state of ROMHM bit
0x8000 – 0xBFFF	Paged FLASH	256K bytes	16 – 16K pages
0xC000 – 0xFEFF	Fixed Flash	16K bytes	
0xFF00 – 0xFFFF	Vectors	256 bytes	BDM if active

*NOTE: The bottom 1K of EEPROM is covered by registers out of reset***.**

Table 3: XDT512 Memory Map

0x0000 – 0x07FF	Registers	2 K bytes	
0x0800 – 0x0BFF	Paged EEPROM	4K bytes	4 – 1Kb pages
0x0C00 – 0x0FFF	Fixed EEPROM	1K bytes	
0x1000 – 0x1FFF	Paged RAM	20 KB	5 – 4Kb pages
0x2000 – 0x3FFF	Fixed RAM	8K bytes	
0x4000 – 0x7FFF	FIXED FLASH	16 KB	1K, 2K, 4K, 8K Protected Boot Sector
0x8000 – 0xBFFF	Paged FLASH	512K bytes	32 – 16Kb pages
0xC000 – 0xFEFF	FIXED FLASH	16 KB	2K, 4K, 8K, 16K Protected Boot Sector
0xFF00 – 0xFFFF	Vectors	255 bits	

INTEGRATED BDM

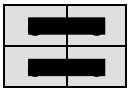
The APS12 board features an integrated Turbo BDM Light (TBDML) based on the Freescale MC9S08JB16 MCU. The integrated TBDML supports application development and debugging via background debug mode and provides primary power to the development module. CodeWarrior development tools fully supports the integrated TBDML BDMy.

The integrated TBDML provides power and ground to the target board eliminating the need to power the board externally. Power from the TBDML is derived from the USB bus. The integrated TBDML is designed to provide a maximum of 300mA of current from the USB bus. Therefore, total current consumption for the target board, and connected circuitry, **must not exceed 300mA**. This current limit describes the current supplied by the USB cable to the BDM circuit, the target board, and any connected circuitry. Excessive current drain will violate the USB specification causing the bus to disconnect. Damage to the host PC USB hub or the target board may result.

BDM_EN HEADER

The BDM_EN header allows the user to connect and disconnect the integrated TBDML to the target MCU. When installed, the integrated TBDML may be used to program and debug application code during development. These option jumpers should be removed for normal operation or when powered externally. If powered externally, the TBDML output drivers may load the output signals excessively.

Figure 2: BDM_PORT



	ON	OFF
BKG	BKGD Enabled	BKGD Disabled
RST	RST Enabled	RST Disabled

NOTE:

Remove both BDM_EN option jumpers if the target boards is not powered from the integrated BDM. This will prevent the unpowered BDM from loading the RESET* signal.

BDM_PORT HEADER

A 6-pin BDM port header allows connection of a HC(S)12 compatible BDM cable for application development. Refer to the BDM cable documentation for details on use of the BDM cable with this module.

Note: The BDM_PORT header is not installed in default configurations.

EXPANDED MODE OPERATION

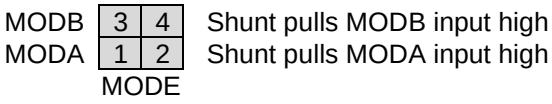
Expanded mode operation is supported only for the APS12C128SLK and the APS12DT256SLK modules. All signals necessary to implement the multiplexed bus are available at connector J1.

The MODE option header is used to configure the module for expanded bus mode operation. Refer to the 9S12DT256 Reference Manual for details on implementing the expanded bus.

MODE

By default, the microcontroller is configured for single-chip operation. The MODE option header allows the user to configure the board for expanded bus operation. In default configuration, this header is not installed.

Figure 3: MODE Option Header



NOTE: Expanded bus mode operation is supported only when a 9S12C128 or 9S12DT256 MCU is installed.

NOTE: The Mode option header is not installed in default configurations.

POWER

There are multiple methods to apply power to the application module. Power may be applied to the board from the integrated USB BDM, through a 2.0mm barrel connector, or through connector J1. The following section describes the various power options and proper configuration.

CAUTION

Damage to the board may result if power is applied from multiple sources.

Power via the MCU_PORT connector

(when connected to Freescale Project Board [PBMCUSLK])

The application module is designed to be used with and powered from the PBMCUSLK. The application module will source power from the PBMCUSLK through connector J1. Refer to the PBMCUSLK User Guide for details on configuring power options for the PBMCUSLK.

Refer to Figure 4 below for details on configuring power input APS12 application module.

Power via the application module integrated USB

This module is designed to draw power from the integrated USB BDM. This supports quick and easy application development and debug. The BDM is configured to provide 300mA of power to the module from the USB bus. The user must ensure this limit is not exceed; otherwise, the host PC will disconnect the USB bus forcing a target device reset. Damage to the module or the host PC may also result. Total power consumption must include the module and any external circuitry connected to the IO header at J1.

Refer to Figure 4 below for details on configuring power input APS12 application module.

Power via the application module barrel connector

The on-board voltage regulator (VR1) accepts power input through a 2.1mm, center-positive, barrel connector (PWR). Input voltage may range from +6V to +18V. The voltage regulator (VR1) provides a +5V fixed output voltage with current output limited to 250mA. Over-temperature and over-current limit built into the voltage regulator provides protection from excessive stresses. Do not exceed the maximum output current limit of VR1 when attempting to power off-board circuitry through connector J1.

Refer to Figure 4 below for details on configuring power input APS12 application module.

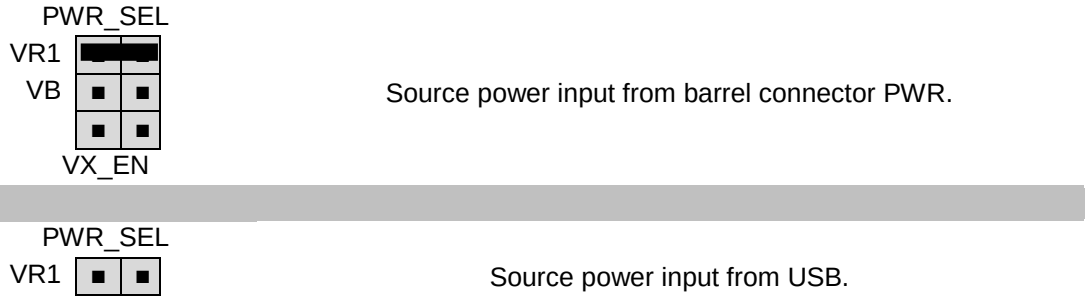
POWER SELECT

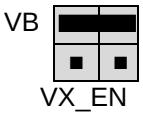
Power may be applied to the board from the integrated USB BDM, through a 2.1mm barrel connector, or through connector J1. Optionally, power may be routed through connector J1 to supply external circuitry. Power selection is achieved by using a 4-pos selection header. When attached to the PBMCUSLK, power is provide by the project board through connector J1.

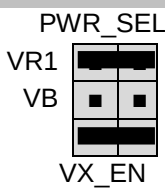
Use caution when configuring this selection header. Applying power to the module through the on-board regulator and connector J1 at the same time may cause damage to the module.

PWR_SEL

Figure 4: PWR_SEL Option Header







Source power from barrel connector PWR and supply power to external circuitry connected to J1.

NOTE: Exercise caution when configuring this selection header. Improper configuration may damage the module.

RESET Switch

The RESET switch provides a method to apply an asynchronous RESET to the MCU and is connected directly to the RESET* input on the MCU. Pressing the RESET switch applies a low voltage level to the RESET* input. Pressing the reset switch causes the reset supervisor at LV1 to assert RESET for 150 ms. A pull-up bias resistor allows normal MCU operation. Shunt capacitance ensures an adequate input pulse width and debounces the RESET switch.

Low Voltage RESET

A DS1813, low-voltage supervisor at LV1 protects the application module under-voltage conditions. LV1 asserts RESET when the 5V rail falls below the trip point of 4.62V. The LV1 RESET output remains asserted for approximately 150ms after voltage returns to nominal.

TIMING

Timing input to the MCU is provided by a 4 MHz, crystal oscillator. The oscillator exhibits a frequency tolerance of ±30ppm. The timing input is configured for full-swing Pierce mode operation in all MCU configurations.

The XCLKS output is routed to test point VIA located near the MCU. The internal clock ECLKX2 is available at this via if needed.

COMMUNICATIONS

The application module provides the user with 1 COM port and 1 CAN port on the module. COM1 is linked to SCI0 on the MCU. The RS-232 channel is configured as a DCE device. This allows a straight through cable between the module and the host PC.

Also, the MCU supports up to 2 additional CAN ports, 2 SPI ports, and 1IIC port depending on the MCU installed. Access to these communications ports is provided through connector J1. Physical layer support is not provided for this feature and must be provided by the user if needed. Refer to the relevant MCU Reference Manual for details

RS-232

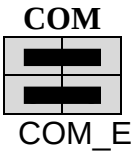
An RS-232 physical-layer transceiver (PHY) provides RS-232 to TTL/CMOS logic level translation on the COM connector. The COM connector is a 9-pin Dsub, right-angle connector. A ferrite bead on shield ground provides conducted immunity protection. Communication signals TXD and RXD are routed from the transceiver to the MCU. Communications signals TXD and RXD also connect to general purpose Port S signals on the MCU. Access to logic signals RTS and CTS are provided by vias located adjacent to the RS-232 PHY at U2.

Table 4: COM Connections

MCU Port	COM Signal	I/O PORT CONNECTOR
PS1/TXD0	TXD0	J1-5
PS0/RXD0	RXD1	J1-7

Communications signals TxD/RxD also route to connector J1 for use off-module if desired. When using these signals to drive off-module RS-232 devices the user should disconnect the on-board RS-232 transceiver. The COM_EN header block allows the user connect or disconnect the RS-232 transceiver.

Figure 5: COM_EN Header



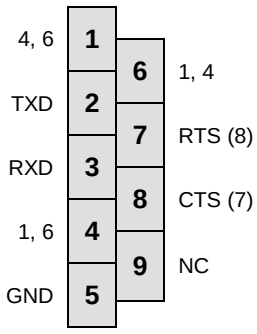
Selects and enables serial communications through COM connector. Remove jumpers to disable on-board RS-232 transceiver.

NOTE: At this time the USB jumpers are not available and therefore no pins are connected to these signals.

COM Connector

A standard 9-pin D-sub connector provides external connection for COM1. The D-sub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. The figure below details the DB9 connector.

Figure 6: COM Connector



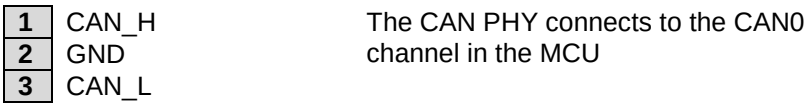
Female DB9 connector that interfaces to the MCU internal SCI0 serial port via the RS232 transceiver. It provides simple 2 wire asynchronous serial communications without flow control. Flow control is provided at test points on the board. A straight-through cable is used to connect the module to a DTE device such as a host PC.

Pins 1, 4, and 6 are connected together.
Pins 7 and 8 are connected together.

MSCAN

The application module provides one PCA82C250 high-speed CAN physical interface. A 3-pin connector provides connectivity to the off-board CAN bus. The CAN PHY connects to the CAN0 channel on the MCU. The PHY supports data rates up to 1 Mbps with slew-rate control. The figure below shows the pin-out of the CAN_PORT connector.

Figure 7. CAN_PORT Connector



The installed MCU may provide support for additional CAN channels. All CAN channels supported are routed to the connector J1 for use if needed. Consult the Reference Manual for the installed MCU for further details.

VRH/VRL

MCU inputs VRH and VRL provide the upper and lower voltage reference for the analog to digital (ATD) converter. By default, VRH is tied to VDD and VRL is tied to ground. Adequate filtering has been added to provide a voltage reference with minimal ripple. Either, or both, references may be isolated to provide alternate ATD input references. A test point via on each signal, labeled VRH, or VRL, provides an easy way to attach an alternate reference voltage.

A 0-ohm configuration resistor allows isolation of each reference voltage. Removing R6 isolates VRH while removing R7 isolates VRL. Install suitably sized 0-ohm resistors in these locations to restore the board to its default configuration.

Care must be exercised when using alternate input references. The associated configuration resistor must be removed before applying an alternate voltage reference or the board may be damaged. Also, no input protection is provided; incorrect configuration will damage the MCU. The table below summarizes the changes necessary to use alternate VRH and/or VRL.

Table 5: ATD Reference Voltage

	Installed (Default)	Removed
R6	VRH = VDD	VRH provided by user
R7	VRL = GND	VRL provided by user

NOTE: Damage to the board may result if an alternate reference voltage is attached without first removing the associated configuration resistor.

USER I/O

User I/O includes 2 push button switches, one 4-position DIP switch, 4 green LEDs, a potentiometer, and a photo-sensor. The sections below provide details on each User I/O. The User option header block enables or disables each User I/O individually.

Switches

The application module provides 2 push button switches and one 4-position DIP switch for user input. Each push button switch is an active low input. The user must enable the internal pull-up bias before using the switch input.

Each DIP switch position is an active low input. Use of the DIP switches requires enabling the associated PORTB pull-ups internal to the MCU to prevent indeterminate input conditions. Table 6 shows the associated connection signal for each switch. Table 7shows the associated USER enable position to enable each switch.

LED's

The application module provides 4 green LEDs for output indication. Each LED is connected to an active low output on the MCU. A current-limit resistor prevents excessive diode current. Table 6 shows the associated connection signal for each LED. Table 7 shows the associated USER enable position to enable each LED.

POT

A single-turn, 5K ohm trimmer potentiometer (POT) has been provided for analog input simuation. The part is decoupled to minimize noise during adjustment. The POT connects to analog input PAD05/AN05 on the MCU. Table 6 shows the associated connection signal for the POT. Table 7 shows the associated USER enable position to enable the POT.

Photo-Sensor

A 4mm photocell light sensor exhibiting 23K – 33K ohms of output resistance has been provided. Output resistance is inversely related to incident light intensity. A gain stage (U5) amplifies the sensor output before connecting to the MCU. The SENSOR connects to analog input PAD04/AN04 on the MCU. Table 6 shows the associated signal connection for the sensor. Table 7 shows the associated USER enable position to enable the sensor.

MCU Signals

The following table shows the connection for each user I/O device. Signals in **BOLD** indicate port functions which are not common to all MCU families supported by the APS12 application module. Refer to the relevant Reference Manual for further details.

Table 6: User I/O

USER	Ref Des	Signal	Description
1	SW1	PP0/KWP0/PWM0/MISO1	Push Button Switch 1 (SW1)
2	SW2	PP1/KWP1/PWM1/MOSI1	Push Button Switch 2 (SW2)
3	SW3-1	PB0/**ADDR0/DATA0**	DIP Switch 1 (DIP-SW1)
4	SW3-2	PB1/**ADDR1/DATA1**	DIP Switch (DIP-SW2)
5	SW3-3	PB2**ADDR2/DATA2**	DIP Switch (DIP-SW3)
6	SW3-4	PB3/**ADDR3/DATA3**	DIP Switch (DIP-SW4)
7	LED1	PB4/**ADDR4/DATA4**	Green LED (LED1)
8	LED2	PB5/**ADDR5/DATA5**	Green LED (LED2)
9	LED3	PB6/**ADDR6/DATA6**	Green LED (LED3)
10	LED4	PB7/**ADDR7/DATA7**	Green LED (LED4)
11	RV1	PAD05/AN05	Potentiometer (RV1)
12	RZ1	PAD04/AN04	Light Sensor (RZ1)

***Not all signals are available for all microcontrollers. Those that may be affected by this are marked in *italic bold.*

User Option Enables

The User option header block enables or disables each User I/O device individually. User I/O includes 4 green LEDs, 2 push button switches, one 4-position DIP switch, a Light Sensor, and a potentiometer. Installing a shunt enables the associated option. Removing a shunt disables the associated option. The table below shows the configuration option for each USER I/O.

Table 7: USER Option Header

			Shunt		
	USER		Installed	Removed	Description
SW1	**1**	**2**	Enable	Disable	Push Button Switch 1 (SW1)
SW2	**3**	**4**	Enable	Disable	Push Button Switch 2 (SW2)
SW3-1	**5**	**6**	Enable	Disable	DIP Switch 1 (DIP-SW1)
SW3-2	**7**	**8**	Enable	Disable	DIP Switch 2 (DIP-SW2)
SW3-3	**9**	**10**	Enable	Disable	DIP Switch 3 (DIP-SW3)
SW3-4	**11**	**12**	Enable	Disable	DIP Switch 4 (DIP-SW4)
LED1	**13**	**14**	Enable	Disable	Green LED (LED1)
LED2	**15**	**16**	Enable	Disable	Green LED (LED2)
LED3	**17**	**18**	Enable	Disable	Green LED (LED3)
LED4	**19**	**20**	Enable	Disable	Green LED (LED4)
RV1	**21**	**22**	Enable	Disable	Potentiometer (RV1)
RZ1	**23**	**24**	Enable	Disable	Light Sensor (RZ1)

MCU I/O PORT

Connector J1 provides access to the microcontroller I/O signals. The figures below show the pin-out for the MCU I/O connector. Only signal XCLS is not available at connector J1.

Signals marked in **BOLD** in the table below are not available on all MCUs supported by the APS12 application module. Refer to the relevant Reference Manual for details.

Figure 8: Connector J1

V_{AUX}	1	2	PE1/IRQ*
GND	3	4	RESET*
PS1/TXD0	5	6	MODC/BKGD
PS0/RXD0	7	8	PP7/KWP7/PWM7/SCK2
PP0/KWP0/PWM0/MISO1	9	10	PAD07/AN07
PP1/KWP1/PWM1/MOSI1	11	12	PAD06/AN06
PT0/IOC0	13	14	PAD05/AN05
PT1/IOC1	15	16	PAD04/AN04
PM4/RXCAN2/RXCAN0/RXCAN4/MOSI0	17	18	PAD00/AN00
PM2/RXCAN1/RXCAN0/MISO0	19	20	PAD01/AN01
PM5/TXCN2/TXCAN0/TXCAN4/SCK0	21	22	PAD02/AN02
PM3/TXCAN1/TXCAN0/SS0*	23	24	PAD03/AN03
PA7/***ADDR15***/***DATA15***	25	26	PJ7/KWJ7/TXCAN4/SCL0
PA6/***ADDR14***/***DATA14***	27	28	PJ6/KWJ6/RXCAN4/SDA0
PA5/***ADDR13***/***DATA13***	29	30	PP2/KPP2/PWM2/SCK1
PA4/***ADDR12***/***DATA12***	31	32	PP3/KWP3/PWM3/SS1*
PA3/***ADDR11***/***DATA11***	33	34	PP4/KWP4/PWM4/MISO2
PA2/***ADDR10***/***DATA10***	35	36	PP5/KWP5/PWM5/MOSI2
PA1/***ADDR9***/***DATA9***	37	38	PS2/RXD1
PA0/***ADDR8***/***DATA8***	39	40	PS3/TXD1
PB7/***ADDR7***/***DATA7***	41	42	PE0/XIRQ*
PB6/***ADDR6***/***DATA6***	43	44	PE2/***RW***
PB5/***ADDR5***/***DATA5***	45	46	PE3/***LSTRB****
PB4/***ADDR4***/***DATA4***	47	48	PE4/***ECLK***
PB3/***ADDR3***/***DATA3***	49	50	PT2/IOC2
PB2/***ADDR2***/***DATA2***	51	52	PT3/IOC3
PB1/***ADDR1***/***DATA1***	53	54	PT4/IOC4
PB0/***ADDR0***/***DATA0***	55	56	PT5/IOC5
PM1/TXCAN0/***TXB***	57	58	PT6/IOC6
PM0/RXCAN0/***RXB***	59	60	PT7/IOC7

Support

For easy answers to your questions, and to get the most out of your support experience, Freescale recommends that you use these resources in the following order:

For frequently asked questions (FAQs), latest updates, and listing of known bugs and solutions.	www.freescale.com\universityprograms OR www.axman.com\support
Ask your questions to our online developer community	www.freescale.com\forums
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