MPC567XADAT516

Demonstration Module Hardware User Guide

Applies to Freescale
MPC5674F & MPC5676R
Microcontrollers

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REVISION

Date	Rev	Comments
November 3, 2008	A	Initial Release – Applies to Rev A only.
October 12, 2009	B	Updated for Rev B. Updated figure and page numbers
January 22, 2010	C	Corrected XTAL frequency, updated 1st page footer
June 4, 2010	D	Corrected JP designators and updated configuration text. Added SRAM section
January 11, 2011	E	Updated for use with MPC5676R MCU
March 16, 2011	F	Added device orientation diagram. Updated development port description
March 17, 2011	G	Corrected NEXUS connector pin-out. Updated MDO Option header section

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be applied whenever handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing reserves the right to make changes without further notice to any products to improve reliability, function or design. Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the MPC567XADAT516 board:

   a) This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

Signal names followed by an asterisk (*) denote active-low signals.

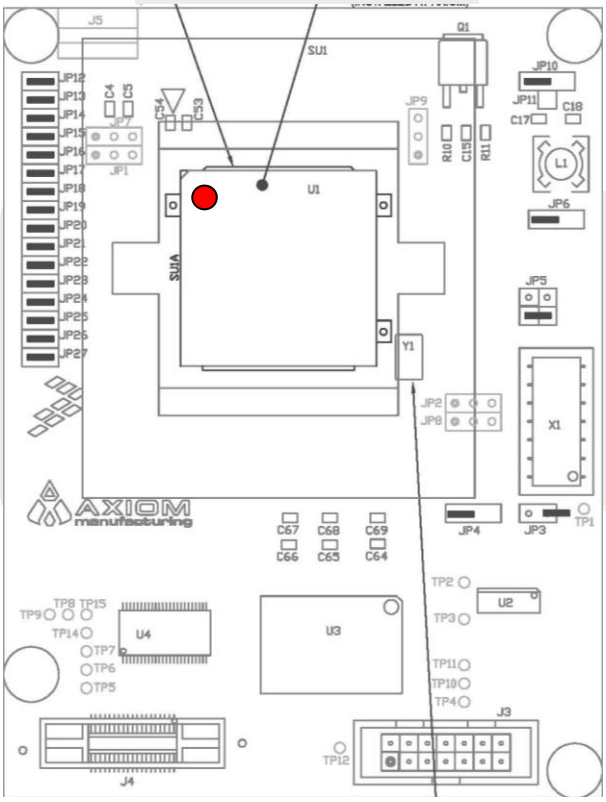
OVERVIEW

The MPC567XADAT516 (ADAT516) supports the MPC5674F and MPC5676R microcontrollers in the 516BGA package. The ADAT516 is a daughter-card type module which is designed to mount directly to the MPC567XEVBMB (EVBMB) via 4, low-profile stack headers. This document details the hardware configuration only for the ADAT516. Refer to the MPC5674 or the MPC5676 Reference Manual (RM) for use and configuration of different MCU options.

DEVICE ORIENTATION

The ADAT416 module applies an open-top socket to allow the target device to be installed and removed easily. However, the socket obscures the pin 1 marking showing device orientation. Although present, the pin 1 marking on the socket is not readily visible. The figure below illustrates the correct device orientation. The solid circle marks the target device pin 1 location.

Figure 1: Device Orientation



POWER SUPPLY

Primary power to the ADAT516 is provided through the stack headers. Alternate power input may be applied through the power input at location J5. Location J5 is designed to accept 3.5mm terminal block. This terminal block is not installed in the default configuration.

Alternate power input allows the ADAT516 to be used as a stand-alone development module.

The MCU VDD input is generated on-board using either a linear pass transistor at Q1 or a switch-mode power supply regulator at Q2. Option headers JP8 (REGSEL) and JP9 (REGCTL) select either the linear regulator or the switch-mode regulator. Refer to the target device Reference Manual for details on use and configuration of the Linear Regulator or the SMPS.

CAUTION: Power to the EVBMB must be disconnected prior to installing the ADAT516. Damage to the ADAT516 and EVBMB may otherwise occur.

Analog Supply

Analog voltage (+5VA) to the ADAT516 is provided from the EVBMB via the 4 board stack headers. This voltage is not generated on the ADAT516 module. VRH_EN connects to +5VA by default. A cut-trace, at CT6, enables this option by default and the jumper is not installed in default configurations.

Analog voltage, +5VA, is not available with the module powered as a stand-alone module. A test point at VRH allows the user to apply different analog voltage input if required. If used in stand-alone mode, the user must apply alternate analog voltage input.

OPTION JUMPERS

The MPC567XADAT516 applies a socket to accommodate the target MCU. Because of this, most option headers are configured for default operation with an embedded cut-trace on the bottom layer. To modify operation of any option header, simply open the cut-trace and add a jumper wire to select the desired option.

Rev C boards have all option headers installed with option jumpers set to default configurations providing maximum configuration flexibility.

The following sections describe the functionality of each option jumper from a hardware standpoint only. Refer to the MPC5674 Reference Manual for further details on use and configuration.

VDDEH_SEL – JP1

The VDDEH_SEL option jumper selects the high-voltage input applied to the target MCU. All target MCU VDDEH inputs are supplied by this option jumper.

Rev C	option jumper is set to +5V by default.
Others	cut-trace selects +5V input by default. This option jumper is not installed.

EXTAL – JP2

The EXTAL_SEL option jumper selects between the on-board, 40 MHz XTAL or the oscillator socket for timing input to the target MCU.

Rev C	option jumper selects XTAL input by default.
Others	cut-trace selects XTAL input by default. This option jumper is not installed in default configurations.

OSC_EN - JP3

The JP3 option jumper applies +3.3V power to the OSC socket at X1. This option jumper is populated in all configurations.

All	option jumper set to OFF by default.

SRAM_SEL – JP4

The SRAM_SEL option jumper selects the MCU chip-select output for use with on-board SRAM memory. This provides the user with greater design memory-map flexibility. This option jumper is installed in all configurations.

All	option jumper selects CS0* input by default.

VDDSYN_EN– JP5

The VDDSYN_EN option jumper allows the end-user to select the source of VDD33 input to the target MCU.

Rev C	option jumper selects MCU VDDSYN output by default.
Others	cut-trace selects MCU VDDSYN output by default. This option jumper is not installed in default configurations.

VDDREG_SEL– JP6

The VDDREG_SEL option jumper connects either +5V or +3.3V to the VDDREG input on the target MCU. This option is installed in all configurations.

All Revs option jumper selects +5V input by default.

VSTBY_SEL– JP7

The VSTBY_SEL option jumper enables or disables internal memory stand-by voltage to the target MCU. By default, this option is configured to disable VSTBY. This option jumper is not installed in default configurations.

Rev C option jumper connects VSTBY input to GND by default.

Others cut-trace connects VSTBY input to GND by default. This option jumper is not installed in default configurations.

REGSEL– JP8

The REGSEL option jumper enables either the on-chip linear regulator controller or the on-chip switch-mode power supply controller.

Rev C option jumper selects linear regulator by default.

Others cut-trace or wire mod enables linear regulator by default.

REGCTL– JP9

The REGCTL option jumper selects between the on-board linear regulator and the on-board switch-mode power supply.

Rev C option jumper selects linear regulator by default.

Others cut-trace or wire mod enables linear regulator by default.

VDDSEL – JP10 / JP11

The VDDSEL option jumper selects source of input VDD applied to the MCU. Input sources include; on-board linear regulator, on-board SMPS, external +1.2V. Input voltage options are mutually exclusive, preventing the user from applying input voltage from several sources. These option headers are applied in all configurations.

All Rev's option jumper set to select on-board linear regulator input by default.

MDO Option Header – JP12 thru JP27

Option headers JP12 – JP27 provide access to Message Data Out signals, MDO[15:0]. MDO signals are associated with the Nexus Development Interface (NDI) and are used to upload Nexus messages on the rising edge of MCKO. Refer to the target device Reference Manual (RM) for details on configuration and use of these signals.

This option header enables and disables MDOx signal connection to the board stack connector at P1 only. MDOx signal connections to the NEXUS Port connector are always active.

SRAM

The ADAT516 is designed to accept several different sizes SRAM memory. The installed part provides 4Mb (128K x 32) of storage in a CY7C1338 SRAM device from Cypress Semiconductor. This family of parts allows installation of memory up to 72Mb (2M x 36). Larger devices also provide 1 parity bit per bank. Parity is not supported by the installed memory device.

SRAM accesses are configured as 32-bit wide, linear burst addressing. The target MCU applies a non-multiplexed bus for the lower 16 address and data bits and multiplexes the upper 16 address and data bits to conserve pins. The ADAT516 board applies an external latch for the upper address bits for providing 32-bit addressing. The board supports chip-select input control using either CS0* or CS1*. This option provides flexibility to the user during applications development. See SRAM_SEL – JP4 above for selection details.

Refer to the MPC5674F or MPC5676R Reference Manual and the CY7C1338 datasheet for details on use and configuration of SRAM and chip-selects.

The installed SRAM device provide 4 Mb of storage arranged as 128K addresses by 32 bits. Accesses to the installed device use address A[13:29] (A13 downto A29). Larger devices will utilize address up to and including A[9:29].

Figure 2: SRAM Options

Capacity	Address	Parity
4Mb, 128K x 32	A[13:29]	None
9Mb, 256K x 26	A[12:29]	0
18Mb, 512K x 36	A[11:29]	0
36Mb, 1M x 36	A[10:29]	0
72Mb, 2M x 36	A[9:29]	0

NOTE: ADAT516, Rev B boards do not support burst mode addressing.
Burst mode addressing is fully supported on Rev C and later boards.

DEVELOPMENT PORTS

The ADAT416 applies 1 NEXUS and 1 JTAG development ports. Several signals are shared by both development ports; therefore, only 1 type of development cable should be applied during any given development session. A CBTLV3861 device buffers development port input and power signals protecting the target MCU from damage by transient input. This buffer provides 5 ohms, series resistance on the development signals when connected. The buffer also provides signal isolation when disconnected.

To ensure proper communications, the ADAT416 and development cable must be powered in the proper sequence. Use the following power sequence to connect a development cable.

The power sequence shown below should be used when connecting a development cable to the ADAT416. This sequence should be used if the ADAT416 is mated to the EVBMB or used in a stand-alone configuration.

ADAT516 Power Sequence

1) Ensure power is switched OFF
2) Connect development port cable to the desired development port
3) Apply power to the target board.
4) If power is removed or the ON-OFF switch is turned off, remove development cable from board connector and re-apply from step 1 of this procedure.

NEXUS Port

The device microcontroller contains multiple Nexus clients that communicate over a single IEEE-ISTO 5001™-2003 Nexus class 3, combined JTAG IEEE 1149.1/auxiliary out interface. Combined, all of the Nexus clients are referred to as the Nexus development interface (NDI). Class 3 Nexus allows for program, data, and ownership trace of the microcontroller execution without access to the external data and address buses.

The MDO Option Header is also associated with the NDI (see above). Refer to the target device Reference Manual for details on configuration and use of the NDI. The development tool port consists of an AMP 38-pin Mictor connector (pn 767053-1). The figure below details the pin-out for the Nexus development tool connector.

Figure 3: NEXUS Port

Signal			Signal
MDO12	1	2	MDO13
MDO14	3	4	MDO15
MDO9	5	6	ENGCLK
BOOTCFG1	7	8	MDO8
B_RESET*	9	10	B_EVTI*
TDO	11	12	B_+3.3V
MDO10	13	14	B_RDY*
B_TCK	15	16	MDO7
B_TMS	17	18	MDO6
B_TDI	19	20	MDO5
B_JCOMP	21	22	MDO4
MDO11	23	24	MDO3
RSTOUT*	25	26	MDO2
NXS27(2)	27	28	MDO1
NXS29(2)	29	30	MDO0
+V	31	32	EVTO*
+V	33	34	MCKO
NXS35(3)	35	36	MSEO1*
B_VSTBY	37	38	MSEO0*

Notes:
1) B_… signals are buffered, bi-directional IO
2) NXSxx signals connect to a test pad adjacent to the NEXUS port connector
3) Signal names followed by a “*” symbol are active logic low.

JTAG Port

The JTAG port provides a standard 1149.1-2001 JTAG connection to the target MCU. The connector is a standard 2x7, 0.1" space, keyed box header. Example compatible cables include the OCDEMON™ NP-JTAG OnCE "Wiggler" and the P&E Microcomputer Systems CABPPCNEXUS. Host software supporting each cable must be used.

The figure below details the pin-out for the JTAG development tool connector.

Figure 4: JTAG Port

Signal			Signal
B_TDI	1	2	GND
TDO	3	4	GND
B-TCK	5	6	GND
B_EVTI*	7	8	JTG8 TP
B-RESET*	9	10	B_TMS
B_+3.3V	11	12	GND
B_RDY*	13	14	B_JCOMP

Notes:
1. B_… signals are buffered.
2. JTG8 TP signal is not connected to the target MCU. This pin connects to a test pad on the board.
3. All development cables may not support the B_EVTI* signal. Option CT5 cut will isolate this signal if not supported by the development cable.
4. Signals followed by a "*" symbol are active- low logic.