CMM-5675

Application Module for Freescale MPC5675K MCU

Hardware User Manual

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Terminology

PPC – Power PC RISC processor technology
EBI – External Data Bus
PDI – Parallel Data Input port
UART – Universal Asynchronous Receiver Transmitter, may be interchanges with SCI
SCI – Serial Communication Interface, may be interchanged with UART
SPI – Serial Peripheral Interface, synchronous 3 or 4 wire serial port
DSPI – SPI with DMA transfer capability
I2C – 2 wire component interconnect, serial interface
TPU – Time Processor Unit, may be a ETPU for enhanced.
ADC – Analog to Digital Converter
ETIMER – enhanced multiple channel timer module.
Flexray – High speed (10Mbps) communication bus similar to CAN bus interface.
CAN – Controller Area Network communication interface.
PWM – Pulse Width Mode, timer operation

Reference Documentation

Reference documents are provided on the Freescale.com MPC5675 product pages and the Axman.com product support pages.

CMM-5675_User_Guide_A.pdf: This user manual. (axman.com)

MPC5675rm.pdf: MPC5675 Device Reference Manual (Freescale)

MPC57675ds.pdf: MPC5675 Data Sheet (Freescale)

Z7drm.pdf: PowerPC z7 core reference manual (Freescale)

CMM-5675_SCH_A.pdf: CMM-5675 board schematics (axman.com)

www.Freescale.com – MPC5675 product pages for application notes, example software, link to Codewarrior software.

www.Pemicro.com – Debug cables, programming software, low cost GUI and GCC tools.

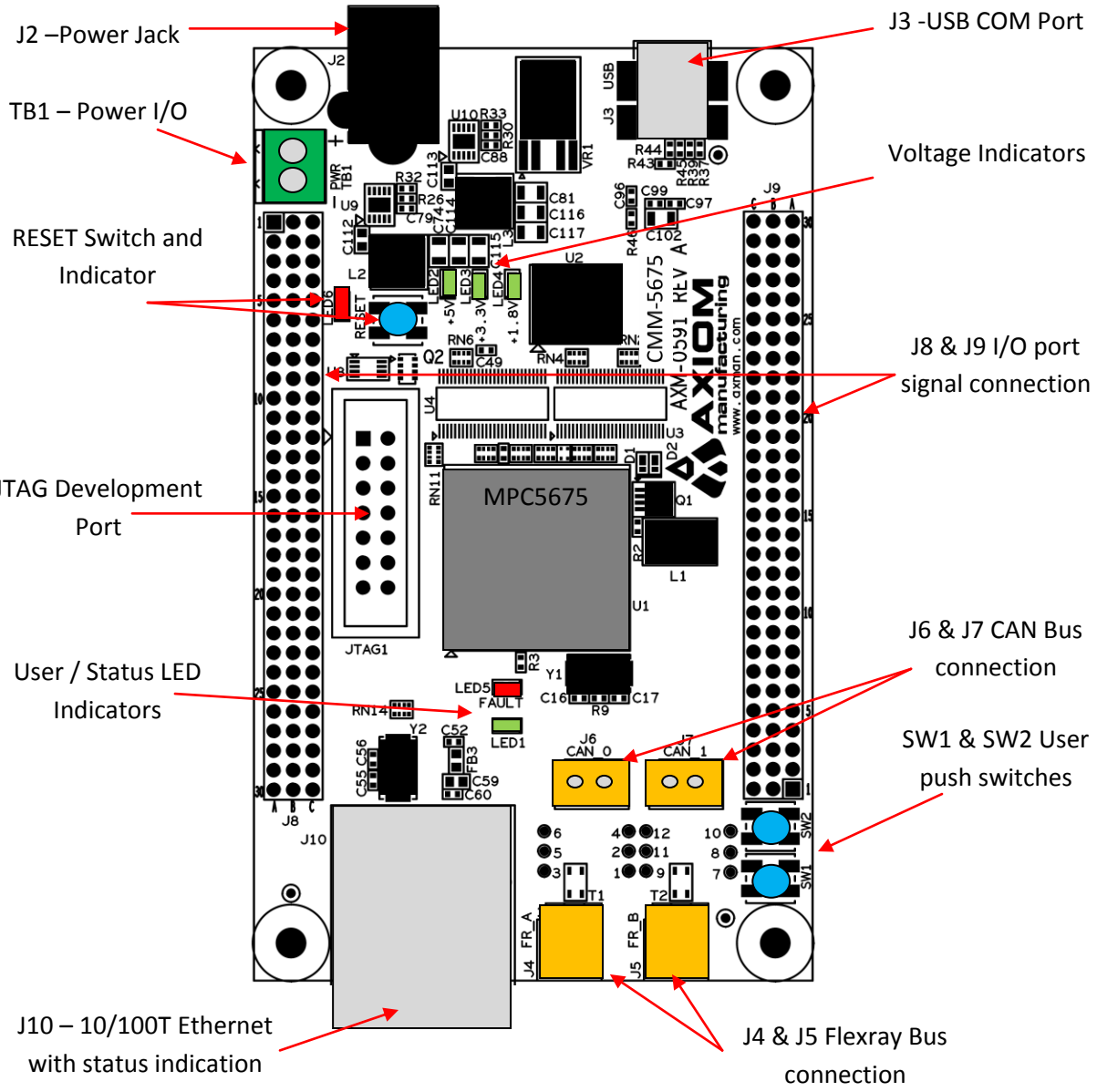
www.lauterbach.com – High end development tools for advanced applications.

CMM-5675 FEATURES

The CMM-5675 is an application or development board based on the Freescale MPC5675 MCU. The MPC5675 device features dual, e200z7d Power Architecture© cores and operates either in Lock-Step Mode for safety-critical applications (IEC 61508 SIL3 compliant) or in Decoupled Parallel Mode for applications requiring maximum performance. The operating mode is selected at boot up time. Software tools from multiple vendors provide a diverse and varied application development and debug eco-system.

The CMM-5675 board provides access to numerous on-chip peripherals; including, CAN, FlexRay, Ethernet, DDR Memory or External Bus peripherals, and UARTs with USB connection. Standard connectors simplify cabling to the CMM-5675 module and stacking capability allows system integration. Many signals and MCU peripherals not applied on-board are accessible on IO headers located along each edge of the module. A 2.1mm barrel connector and optional terminal block make applying power easy.

Module Features:



MPC57675 180Mhz MCU, 473 MAPBGA

- Dual, e200z7d, 32-bit Power Architecture© Processor Cores (PowerPC)
- Instruction clocks up to 180 MHz
- PPS & VLE Instruction Set support
- Safety-Critical Lock-Step Mode or High Performance Decoupled Parallel Mode Operation
- IEC 61508 SIL3 Compatible w/ Lock-Step mode and Fail-Safe Protection
- Device Memory: 512 KB SRAM, 2 MB Code Flash, 64 KB Data Flash
- On-Die Temperature Sensor

External Memory

- DDR and EBI modes supported
- 2GB Mobile DDR on-board, 180Mhz x 16
- Buffered interface for access to EBI signals at IO headers
- Software selectable DDR or EBI interface

Module Power

- On-Board +5V, +3.3V, +1.8V Power Supplies
- Optional, High-Precision Voltage Reference for MCU VREF Input (not populated).
- 2.1mm, center-positive, barrel connector
- 3.5mm, 2-position, Terminal Block
- Reverse Polarity Protection at voltage input

Communications

- 10/100 Mbps Fast Ethernet / MII PHY interface w/ RJ-45 Connector
- 2 ea, FlexRay Transceivers on FRA & FRB; w/ 2-pos, Right-Angle, MicroBlade connectors
- 2 ea, CAN Transceivers on CAN0 & CAN1; w/ 2-pos, Vertical, SPOX connectors
- Dual USB to Serial UART on SCI0 & SCI1
    - Enumerates as 2 Serial COM Ports when connected to a Windows PC
    - Native Windows COM port support
    - USB, mini-B connector
    - Integrated SPI Flash to store Configuration Parameters

Development Port

- 14-pos, JTAG / 1149.1-2001Test Access Port connector, Nexus development and debug

User Application Feature

- User Input Push-Button Switch on GPIO12 / Interrupt capable
- NMI Input Push-Button Switch on NMI input, configurable
- Green LED on GPIO108
- Red LED / FCCU Output Indicator, Exclusive-OR'd to FAULT[1:0] outputs

Expansion Connection

- J8 and J9 MCU Ports
    - 4x 12-bit ADC's, 34 channels total
    - 19-bit, Parallel Digital Interface (PDI), 16-bit Data, 3-bit Control
    - 2 x DSPI Modules, with multiple chip selects
    - FlexPWM timer, multiple channels
    - ETimer, 24 channels
    - EBI data and address bus
    - Other GPIO

Specifications:

Board Size 2.25 x 3.75 Inch, .125 dia. mounting holes, spacing 1.950 x 3.450 inch
Voltage Input: 5.5VDC to 24VDC

GETTING STARTED

The CMM-5675 is provided operating a test application that provides a serial prompt on the USB COM ports. Follow these steps to review the test menu prompt.

1) Carefully unpack the CMM-5675 and observe ESD preventive measures while handling the board.

2) Apply +9V or +12V typical power supply to the CMM-5675 board at the J2 Power Jack or the TB1 power terminal. Follow polarity of connection or damage may occur to the board. See board connector section for specific connection details.

3) Board power indicators should be on when power is applied.

4) Connect USB cable (A to mini-B) from host PC to CMM board J3 USB connector. USB drivers should automatically install on a Windows PC. Two COM ports will be added to the system when the cable is connected to a powered CMM board. Please note the COM port numbers available on the host PC.

5) Open a Serial Terminal software on the host PC. Tera Term or Windows Hyperterminal or similar is needed for communication.

6) Set up the software and select the 2nd COM port added by the CMM board. Settings = 115.2K baud, 8 bit data, 1 stop, and no parity bits.

7) Press the CMM board RESET switch and release. The following prompt should appear on the terminal screen:

```
AXM-0591 (CMM-5675) Diagnostic Program  --  Mar 25 2015

 1 Expansion Connection
 2 Flexray
 3 CAN
 4 Push Switch
 5 LEDs
 6 LAN
 7 EBI - Write Test
 9 DDR Memory

 0 Test All
```

8) Select an option number to perform diagnostic testing. The CMM board is ready to apply for development or loading of another application.

Software Development

Development board users and application developers should also be familiar with the hardware and software operation of the target MPC5675 device. Refer to the Freescale MPC5675 Reference Manual, Data sheet, application notes, and Codewarrior user documentation for in depth details.

The example test diagnostic project may be applied to begin new application projects. Many other drivers and examples are provided by Freescale or by 3rd party tool providers if applied. For full application of the MPC5675 an in-depth knowledge of the device capabilities and features is required. The device is supported by tool and firmware vendors that have developed many powerful applications that may save significant development time for the end user application.

Typical application development is performed by applying the JTAG / Nexus development port with a cable to the host PC to firmware download and run time control. Development debug features for breakpoints, stepping, and memory view / modification are provided for both cores on the one port. Codewarrior and other tools sets provide compiler and debug GUI in one software package. Lower cost / lower feature tools may also be applied.

The target development environment and procedure for best success is to place software to be tested into MPC5675 internal RAM memory or the external DDR memory space. Development tool initialization operations must configure the memory spaces prior to loading of the application to be tested. Review configuration script settings with examples. After the application is tested and operational, flash based initialization is applied with the firmware flashed inot the MPC5675 flash memory space.

The default boot type is from MPC5675 internal flash memory. The MCU ports provide option signal access to change the boot method for the user end application if required (CAN or UART). Refer to the FAB, ABS0 and ABS2 alternate function signals.

CMM-5675 Hardware Description

The CMM-5675 board provides an application module and a basic development platform the MPC5675 microcontroller. No configuration options are provided on the module except the installation of an optional precision reference for the analog converters. All application options are firmware configurable.

Operating mode of the MPC5675 is set at RESET by the internal Boot Assist Module (BAM) for internal flash firmware and unlinked core modes with core 0 operating and core 1 in standby by default. Oscillator clock source is always the internal 16Mhz IRCOSC with PLL enabled at RESET time and any external clocks with operating frequency changes are selected by firmware during initialization.

Lock Step Mode for the dual cores is a shadow flash register configuration operation and must be enabled by flash settings in development mode. Note that lock step mode limits the maximum operating frequency to 90Mhz (180Mhz each core if decoupled).

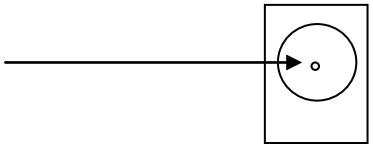
Following are descriptions of the main components and options provided on the board.

POWER SUPPLY

Input power is applied by external connection to the J2 - PWR power jack or the TB1 screw terminal block. The input supply is provided to the main 5V and 3.3V regulators U9 and U10. VR1 provides 1.8V from the 3.3V supply for the DDR memory device. MPC5675 core voltage of 1.2V is self regulated from the +5V supply.

The J2 jack accepts a standard 2.0 ~ 2.1mm center barrel plug connector (positive voltage center) to provide the +VIN supply of +5.5V to +24 VDC (+12VDC typical).

+Volts, 2mm center



TB1 provides 26GA to 18GA wire connection for VIN power access or provide a VIN supply. Observe the + and – terminal markings for voltage polarity.

The J8 MCU I/O port also provides +VIN supply access if module is stacked. Refer to J9 signal chart for details.

Voltage indication for 1.8V, 3.3V and 5V are provided on the module.

ANALOG SUPPLY

The ADC VREF supply is provided by the R/C filtered +5V supply by default. An optional 4.096V voltage reference (VR2 = ADR5044) may be installed for a 1mv ADC resolution. The VREF voltage is applied to all ADC converters in the MPC5675.

RESET

The MPC5675 provides internal Reset status monitoring and output signaling options for application operation. Application configuration may disable the RESET input to the MPC5675.

External reset is provided by the RESET switch, LV1 low voltage detector, JTAG development port, or user applied connection to the RESET* signal on the J9 MCU PORT. If the main 3.3V supply is below operating level, the LV1 voltage detector will set the RESET signal active.

RESET switch provides for manual application of the MPC5675 RESET* signal. Both the RESET switch and LV1 provide a 150ms delay after release for the system to stabilize.

The RESET Indicator will be on during the RESET active condition.

USER INDICATORS

Indication is provided for power supply status, Reset status, Ethernet status, and User application. The indications may be applied to determine proper operation of the CMM board.

Indicator Summary

INDICATOR	COLOR	OPERATION	DEFAULT CONDITION
+5V	Green	+5V power present	ON
+3.3V	Green	+3.3V power present	ON
+1.8V	Green	+1.8V power present	ON
RESET	RED	CPU is in RESET state	OFF
J10 Left = LNK	Green	Ethernet has Link	ON with Network Link, blink with activity
J10 Right = SPD	Yellow	Ethernet is operating 100 base	ON if 100 base network, OFF if 10 base network
LED1	Green	User Application, GPIO108	Off, GPIO108 = 1 to enable.
FAULT	Red	User Application, FAULT1 and FAULT2	Off, FAULT1 or FAULT2 = 1

SWITCHES SW1 and SW2

Push switches are active low level signal output. SW1 provides an optional NMI interrupt input when pressed. SW2 provides the GPIO12 input or an optional interrupt if enabled.

SYSTEM CLOCKS

A reference crystal oscillator of 40Mhz is provided to the MPC5675 for Flexray communication consideration. The external crystal clock may be applied internally to the Flexray module for communication timing requirement. The external clock may also be applied to the internal PLL system clock generation for more precise timing than the internal IRCOSC clock.

External bus clocks are 180MHz maximum for the DDR memory or 45MHz maximum for the EBI clock out.

Memory and External Bus Application

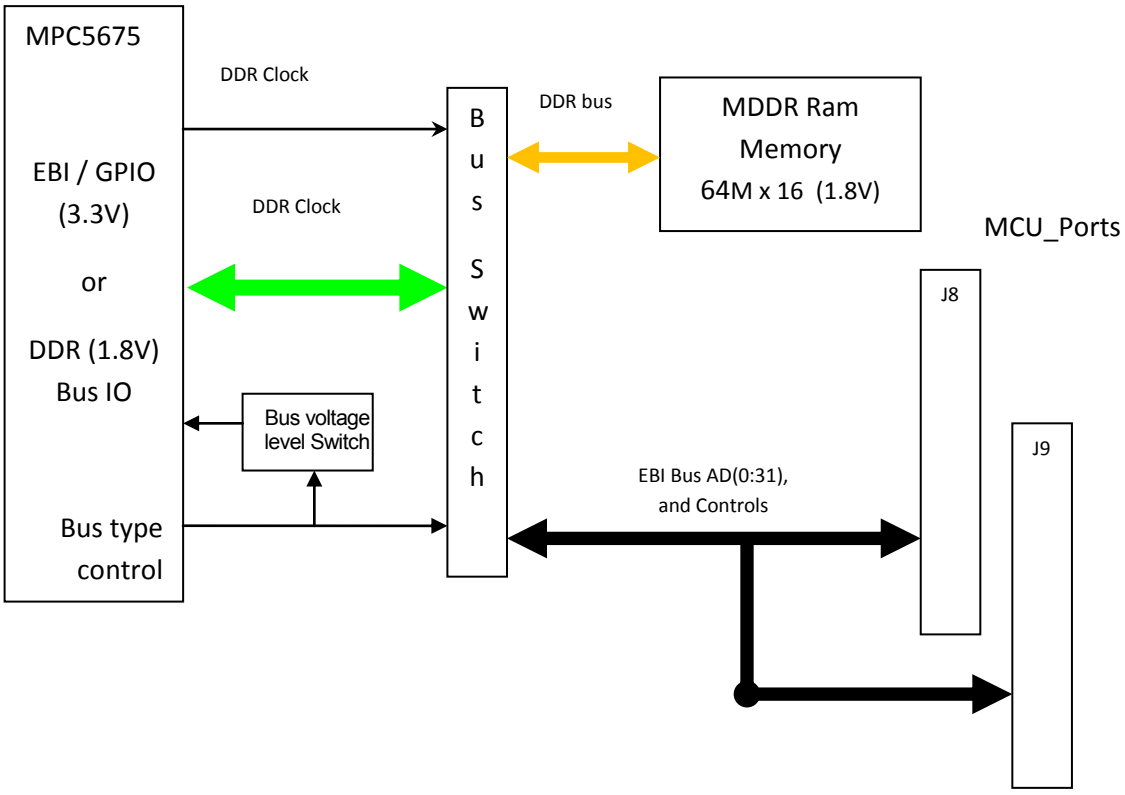
Memory for program storage or nonvolatile data is provided as MPC5675 internal Flash of 2M bytes. The MPC5675 provides 512K bytes of high speed SRAM memory internally.

Board memory consists of a 128M byte mobile DDR2 RAM. External memory may be applied ona host platform for the CMM module and accessed via the EBI data bus.

Memory Device: MDDR Micron MT46H64M16

Note: The MPC5675 DRAM controller must be configured prior to application of the MDDR memory space when BDM or JTAG tools are applied.

External Bus Block Diagram



External Bus Application

The MPC5675 external bus is internally configured to provide a MDDR Memory Bus, EBI local bus, or GPIO and other signals. Only one configuration is valid and the bus type control must be set correctly to support. When MDDR memory is applied, the EBI and GPIO operation is disabled. The two settings change the MPC5675 pin signal level from 1.8V to 3.3V operation under software / firmware control. An external multiplexer provides the signal path control between the lower voltage MDDR memory and the EBI / GPIO signal levels.

Bus Type Control

Two signals provide bus type control for the external memory bus and the default selection is 3.3V GPIO. Software / Firmware must support MDDR bus by correct initialization. EBI bus may be enabled and applied by MPC5675 internal configuration. The following table provides bus type control signals and levels:

Control Signal	MPC5675 Pin: Signals	EBI / GPIO Select	MDDR Select
EBI_ON*	B3: GPIO22 / IRQ18	Low level (Default)	High Level
DDR_ON	B13: GPIO205 / FEC_TXER / DSPI2_CS3	Low Level (Default)	High Level

Port initialization of the MPC5675 is performed in EBI / GPIO mode. DDR mode selection is performed after the MPC5675 DDR bus signals have been enabled followed by DDR memory device initialization and application.

Sequence of bus type mode change:
EBI / GPIO mode = selected anytime DDR is not being accessed.
DDR Mode =

1) EBI Mode enabled with bus type control signals.
2) MPC5675 MDDR mode signals enabled on the bus pins.
3) MDDR Mode enabled with bus type control signals.
4) MDDR device is initialized (may be restored if previously placed in low power refresh mode).
5) MDDR device applied, associated J8 and J9 MCU Port EBI / GPIO signals are tri-stated.

COMMUNICATION PERIPHERALS

The CMM-5675 provides 4 types of media conditioned communication ports: 10/100T Ethernet, USB Serial COM (2 channels of COM), Flexray (2 channels), and CAN (2 channels).

J10 - 10/100T Ethernet

The Ethernet interface is provided by the MPC5675 MAC hosting a Micrel KSZ8041 MII PHY with integrated magnetic RJ45 jack. The RJ45 provides Speed and Link/Active indicators. Speed (Yellow) is ON in 100T mode and off in 10Base mode. Active / Link (Green) will be on and blink off with activity. The LED indication is programmable with the MII Management port.

The KS8041 PHY provides automatic connection type detection. Connection settings maybe set manually by the MII Management port. Refer to the KSZ8041 User Guide and the MPC5675 FEC reference for details.

MPC5675 FEC MII Pin to Signal Reference

MPC5675 PIN	FEC MII Signal	GPIO SIGNAL
B12	RXD0	GPIO211
C14	RXD1	GPIO212
D14	RXD2	GPIO213
B9	RXD3	GPIO214
A9	RXDV	GPIO210
B10	RXERR	GPIO215
C13	RXCLK	GPIO209
B11	TXD0	GPIO201
C11	TXD1	GPIO202
A10	TXD2	GPIO203
A13	TXD3	GPIO204
A12	TXEN	GPIO200
A11	TXCLK	GPIO207
C12	CRS	GPIO208
C15	COL	GPIO206
A10	MDIO	GPIO198
D15	MDC	GPIO199

Note: TXERR / GPIO205 is applied for DDR ON control signal.

J3 – USB COM Port

J3 mini-B USB connection provides a USB 2.0 type connection for the MPC5675 SCI0 and SCI1 UARTs. The physical serial to USB interface is provided by a FTDi FT2232. The device drivers are automatically loaded by most Windows systems. The www.ftdichip.com web sight provides drivers and test utilities. Some custom USB configuration is possible.

The USB COM ports will establish on the host PC as in COM numerical order with SCI1 as the first COM port and SCI0 as the second. Default application of the CMM test utilities applies SCI0 or the 2nd COM port. Refer to the PC System device manager to review COM port assignment.

Note that the USB COM ports will disconnect from the host PC when the CMM board is powered off. Host PC driver load takes several seconds to several minutes depending on the system. COM port selection must be re-established in the Terminal software applied in the case of a COM port disconnect.

MPC5675 SCI Port Pin to Signal Reference

MPC5675 PIN	SCI Signal	GPIO SIGNAL
V20	SCI0 - TXD	GPIO18
W20	SCI0 - RXD	GPIO19
AA22	SCI1- TXD	GPIO94
AB21	SCI1- RXD	GPIO95

J6 and J7 CAN Ports

The CAN ports provide the physical interface layer for the MPC5675 FlexCAN Controller Area Network version 2.0B CAN0 and CAN1 channels. Signal pins from the MPC5675 are connected to a 3.3V CAN transceiver capable of 1M baud communication (SN65HVD230). Transceiver differential CAN network signals CAN_HI and CAN_LO are provided a 120 ohm termination.

The CAN transceiver has CAN signal drive control via the **RS** test pad on the development board. The RS signal is provided a 10K Ohm pull-down resistor to enable the transceiver. The associated transceiver control pin should be applied to enable the transceiver for high speed signaling or to disable. User may refer to the SN65HVD230 data sheet and apply additional signal slope control as needed. The CAN port connectors are Molex SPOX series 2 position, 2.54MM pin spacing.

MPC5675 CAN Port Signal Reference

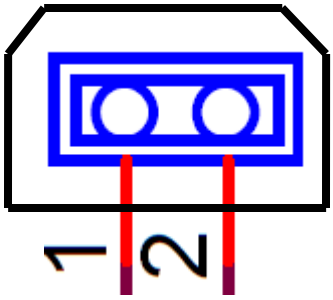
MPC5675 PIN	SCI Signal	GPIO SIGNAL
C20	CAN0- RXD	GPIO17
C21	CAN0- TXD	GPIO16
B5	CAN0_RS	GPIO219 (Output, Low active)
B3	CAN1- RXD	GPIO15
B4	CAN1- TXD	GPIO14
C2	CAN1_RS	GPIO220 (Output, Low active)

Slope adjustment:

CAN0 = R53 (0 ohm default)
CAN1 = R55 (0 ohm default)

J6 and J7 connector Reference

Top View



Pin 1 = CAN_Lo

Pin 2 = CAN_Hi

J4 and J5 Flexray Ports

The MPC5675 provides two independent Flexray controllers that are applied on the CMM board by TJA1080 Flexray media transceivers. Each transceiver provides Flexray bus control and status to the MPC5675. The CMM board provides the primary TX / RX communication signales with the TX enable control. Other transceiver signals for status and network topology must be applied by the user. Refer to the NXP TJA1080 datasheet for more details on status and networking if required.

Each port is filtered and impedance matched to 100 ohm cable. Connector type is Molex Micro Blade 2mm two position connector.

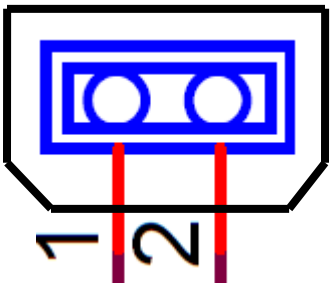
MPC5675 Flexray Pin Signal Reference

MPC5675 PIN	Flexray Signal	GPIO SIGNAL
B8	FR-A- RXD	GPIO48
E3	FR-A-TXD	GPIO49
A8	FR-A- TXEN	GPIO47
J3	FR-A_EN	GPIO217 (Output, active high) w/ pull-up
A7	FR-B- RXD	GPIO51
C5	FR-B- TXD	GPIO50
B7	FR-B- TXEN	GPIO52
J2	FR-B-EN	GPIO218 (Output, active high) w/ pull-up
TJA1080-1 Signal	**Access TP #**	**Comment**
FR-A-RXE_n	TP1	Status - RX signal present output
FR-A-ERR_n	TP2	Status- Error condition output
FR-A-BGE	TP3	Control – Bus Guardian Enable (input w/ pull-up, active high)
FR-A-WAKE	TP4	WAKE input
FR-A-INH1	TP5	Power Control Output
FR-A-INH2	TP6	Power Control Output
TJA1080-1 Signal	**Access TP #**	**Comment**
FR-B-RXE_n	TP7	Status - RX signal present output

FR-B-ERR_n	TP8	Status- Error condition output
FR-B-BGE	TP9	Control – Bus Guardian Enable (input w/ pull-up, active high)
FR-B-WAKE	TP10	WAKE input
FR-B-INH1	TP11	Power Control Output
FR-B-INH2	TP12	Power Control Output

J4 / J5 Connector Reference

Front View



Pin 1 = BP

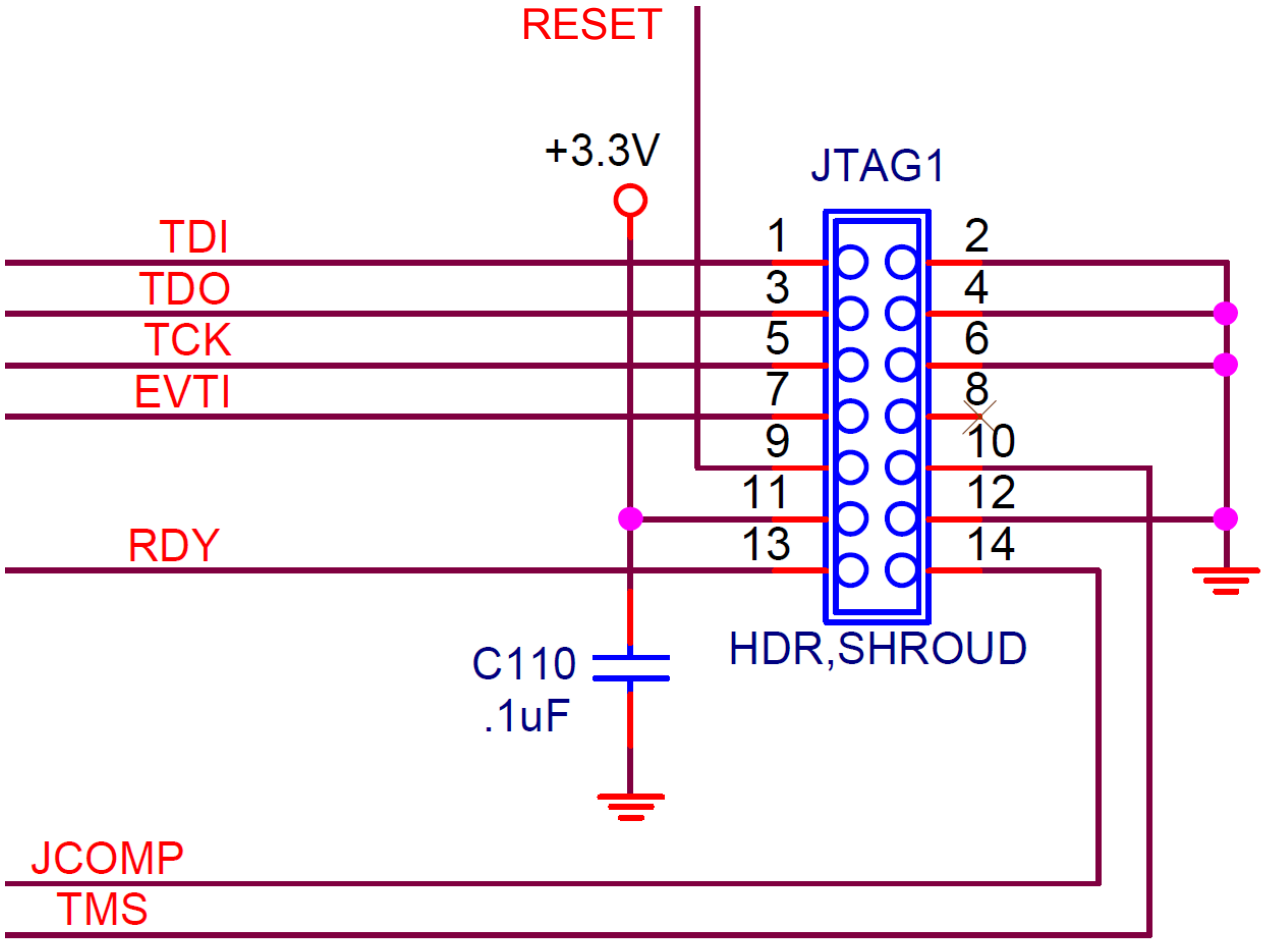
Pin 2 = BM

JTAG Development Port

The JTAG port provides access to the Nexus Development Module in the MPC5675. Port is compliant with standard .1 inch space 2x7 (14 pin) Freescale defined port. Comaptible with PEMicro and other Debugger cables. CMM board does not support real time trace output features of the Nexus development ports due to port connector type.

Nexus MDO12 – 15 signals are applied as GPIO on the CMM board. Debug tool software should apply “Basic” port type configuration in the initialization settings. User application will overwrite these settings but issues may arise if configuration type is not observed. The JTAG Nexus signals applied to the connector are dedicated and do not have an alternate function on the CMM board.

JTAG Port Connection



J8 and J9 MCU Expansion Ports

J8 and J9 provide access and expansion to a majority of MPC5675 I/O signals. The following charts provide detailed reference for the signals available. Special caution should be applied with the EBI and the ADC signals. EBI signals will tri-state when the CMM board MDDR is enabled by the Bus switch controls. The ADC – AN signals provide a maximum input voltage range that depends on the Analog VREF value setting. All other signals are typically 3.3V LVCMOS rated.

Connector type is 3 column 2mm grid. Connectors are not installed by default and may be populated as stack up, stack down, Male header pins, or female socket headers. Samtec supports the triple row connector type in the TW30, SQT30, AND ESQT30 series with various stack options and heights. Axiom can OEM install your connector preference.

J8 Signal Map

Pin #	Row A Signal	Row B Signal	Row C Signal
1	VIN – Power supply I/O	VIN – Power supply I/O	VIN – Power supply I/O
2	Ground	Ground	Ground
3	B_EBI AD0/A16/GPIO166	B_EBI AD1/A17/GPIO167	B_EBI AD2/A18/GPIO168
4	B_EBI AD3/A19/GPIO169	B_EBI AD4/A20/GPIO170	B_EBI AD5/A21/GPIO171
5	B_EBI AD6/A22/GPIO172	B_EBI AD7/A23/GPIO173	B_EBI AD23/GPIO189
6	B_EBI AD22/GPIO188	B_EBI AD21/GPIO187	B_EBI AD20/GPIO186
7	B_EBI AD19/GPIO185	B_EBI AD18/GPIO184	B_EBI AD17/GPIO183
8	B_EBI AD16/GPIO182	B_EBI AD8/A24/GPIO174	B_EBI AD9/A25/GPIO175
9	B_EBI AD10/A26/GPIO176	B_EBI AD11/A27/GPIO177	B_EBI AD12/A28/GPIO178
10	B_EBI AD13/A29/GPIO179	B_EBI AD14/A30/GPIO180	B_EBI AD15/A31/GPIO181
11	B_EBI AD24/GPIO190	B_EBI AD25/GPIO191	B_EBI AD26/GPIO192
12	B_EBI AD27/GPIO193	EBI AD28/FPWM0_X0/GPIO194	EBI AD29/FPWM0_X1/GPIO195
13	EBI AD30/FPWM0_X2/GPIO196	EBI AD31/FPWM0_X3/GPIO197	B_EBI CS0n/FPWM1_B0/GPIO156
14	B_EBI CS1n/FPWM1_A1/GPIO157	B_EBI WBE0n/FPWM0_A2/GPIO151	B_EBI WBE1n/FPWM0_B2/GPIO152
15	B_EBI WBE2n/FPWM0_A3/GPIO153	B_EBI WBE3n/FPWM0_B3/GPIO154	B_EBI OEn/FPWM0_A0/GPIO147
16	B_EBI TEAn/EBI_A11/GPIO161	B_EBI ALE/EBI_A12/GPIO162	B_EBI TAn/EBI_A10/GPIO160
17	B_EBI TSn/FPWM0_B1/GPIO150	B_EBI BDIP/FPWM1_A0/GPIO155	B_EBI CS3n/EBI_A9/GPIO158
18	B_EBI CS2n/EBI_A8/GPIO159	B_EBI A13/FPWM1_B1/GPIO163	B_EBI A14/FPWM1_A2/GPIO164
19	B_EBI A15/FPWM1_B2/GPIO165	B_EBI RW/FPWM0_A1/GPIO149	B_EBI CLKOUT/FPWM0_B0/GPIO148
20	Ground	Ground	Ground
21	PDI_D15/SENS_SEL0/I2C2_DAT/ GPIO146	PDI_D14/SENS_SEL1/I2C2_CLK/ GPIO145	PDI_D13/SENS_SEL2/CTU1_EXT_TGR / GPIO144
22	PDI_D12/GPIO143	PDI_D11/FPWM2_X0/GPIO142	PDI_D10/FWM2_X3/GPIO141
23	PDI_D9/FPWM2_X2/GPIO140	Ground	PDI_LINE/L2_TXD/GPIO129
24	PDI_FRAME_V/GPIO130	PDI_CLK/FPWM2_B1/ET1_ETC3/ GPIO128	PDI_D0/L3_TXD/GPIO131
25	PDI_D1/FPWM2_B3/GPIO132	PDI_D2/FPWM2_A1/ET1_ETC2/ GPIO133	PDI_D3/FPWM2_X1/GPIO134
26	PDI_D4/FPWM2_A2/ET1_ETC4/ GPIO135	PDI_D5/FPWM2_A0/ET1_ETC0/ GPIO136	PDI_D6/FPWM2_B0/ET1_ETC1/ GPIO137
27	PDI_D7/FPWM2_B2/ET1_ETC5/ GPIO138	PDI_D8/FPWM2_A3/GPIO139	Ground
28	CLKOUT2/ET2_ETC5/GPIO233	Ground	ET0_ETC0/GPIO4
29	ET0_ETC1/GPIO1	ET0_ETC2/GPIO2	ET0_ETC3/GPIO3
30	ET0_ETC4/GPIO43	ET0_ETC5/GPIO44	Ground

J9 Signals

Pin #	Row A Signal	Row B Signal	Row C Signal
1	DSPI2_CS2/L3_TXD/CAN2_TXD/GPIO42	DSPI2_CS1/L3_RXD/CAN2_RXD/GPIO9	DSPI1_SIN/EIRQ_8/GPIO8
2	DSPI1_SCK/GPIO6	DSPI1_SOUT/GPIO7	DSPI1_CS0/DSPI0_CS7/GPIO5
3	DSPI1_CS2/DSPI0_CS5/GPIO56	DSPI1_CS3/L2_TXD/ DSPI0_CS4/GPIO55	DSPI2_CS0/CAN3_TXD/GPIO10
4	DSPI2_SCK/CAN3_RXD/GPIO11	DSPI0_SIN/DEBUG7/GPIO39	DSPI0_SCK/DEBUG5/GPIO37
5	DSPI0_SOUT/DEBUG6/GPIO38	DSPI0_CS0/DEBUG4/GPIO36	DSPI0_CS2/I2C2_DAT/GPIO54
6	DSPI0_CS3/I2C2_CLK/GPIO53	Ground	Ground
7	Ground	FPWM0_X0/L2_TXD/GPIO57	FPWM0_X1/GPIO60
8	FPWM0_X2/L3_TXD/GPIO98	FPWM0_X3/GPIO101	FPWM0_F0/DSPI2_SIN/GPIO13
9	FPWM0_A0/GPIO58	FPWM0_A1/GPIO80	FPWM0_A2/GPIO99
10	FPWM0_A3/GPIO102	FPWM0_B0/GPIO59	FPWM0_B1/GPIO62
11	FPWM0_B2/GPIO100	FPWM0_B3/GPIO103	FPWM1_X0/ET2_ETC0/DSPI0_CS1/ GPIO116
12	FPWM1_X1/ET2_ETC1/DSPI0_CS4/ GPIO119	FPWM1_X2/ET2_ETC2/DSPI0_CS5/ GPIO122	FPWM1_X3/ET2_ETC3/DSPI0_CS6/ GPIO125
13	FPWM1_A0/CN2TXD/GPIO117	FPWM1_A1/CN3TXD/GPIO120	FPWM1_A2/GPIO123
14	FPWM1_A3/ET2_ETC4/DSPI0_CS7/ GPIO126	FPWM1_B0/GPIO118	FPWM1_B1/GPIO121
15	FPWM1_B2/GPIO124	FPWM1_B3/ET2_ETC5/GPIO127	Ground
16	Ground	Ground	ADC3_AN0
17	ADC3_AN1	ADC3_AN2	ADC3_AN3
18	ADC2_ADC3_AN11	ADC2_ADC3_AN12	ADC2_ADC3_AN13
19	ADC2_ADC3_AN14	ADC2_AN0	ADC2_AN1
20	ADC2_AN2	ADC2_AN3	ADC0_AN0
21	ADC0_AN1	ADC0_AN2	ADC0_AN3
22	ADC0_AN4	ADC0_AN5	ADC0_AN6
23	ADC0_AN7	ADC0_AN8	ADC0_ADC1_AN11
24	ADC0_ADC1_AN12	ADC0_ADC1_AN13	ADC0_ADC1_AN14
25	ADC1_AN0	ADC1_AN1	ADC1_AN2
26	ADC1_AN3	ADC1_AN4	ADC1_AN5
27	ADC1_AN6	ADC1_AN7	ADC1_AN8
28	N/C	ET1_ETC0/GPIO4	ET1_ETC1/GPIO45
29	ET1_ETC2/CTU0_EXTGR/GPIO46	ET1_ETC3/GPIO92	ET1_ETC4/CTU1_EXTTGR/GPIO93
30	ET1_ETC5/GPIO78	Ground	RESET*

TROUBLESHOOTING

The CMM-5675 is fully tested and operational before shipping. If it fails to function properly, inspect the board for obvious physical damage first. Verify the communications setup as described under GETTING STARTED.

The most common problems are improperly configured options or communications parameters.

1. Verify power indicators are ON. If not, check power connection and supply.
2. Make sure that the RESET* line is not being held low or the RESET indicator is not on constantly.
3. Verify that the USB Port has established a COM port on the Host PC. The 2nd COM port instance is selected and Baud rate is 115.2Kbaud. Verify Terminal software application.
4. Remove USB cable and power from the board and apply power again then the USB.
5. If the BDM cable with development tools has been applied, the board flash may be corrupt or contain unknown firmware. Apply development tool to flash the MPC5675 again or to check application operation.
6. Contact support@axman.com by email for further assistance. Provide board name and describe problem.