MPC5554DEMO

Development Board for the Freescale MPC5554

OPTIONS and CONNECTIONS

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Cautionary Notes

1) Electrostatic Discharge (ESD) prevention measures should be applied whenever handling this product. ESD damage is not a warranty repair item.

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3) EMC Information on the MPC5554DEMO board:

a) This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of CE and the FCC as a **CLASS A** product.

b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

c) In a domestic environment this product may cause radio interference in which case the user may be required to take adequate prevention measures.

d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

Terminology

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be idled by installing on 1 pin so they will not be lost.

This development board applies hardwired option selections (VRL_EN and CUTAWAY 1 – 16). These option selections apply a circuit trace between the option pads to complete a default connection. This type connection places an equivalent Jumper Installed type option. The circuit trace between the option pads maybe cut with a razor blade or similar type knife to isolate the default connection provided. Applying the default connection again can be performed by installing the option post pins and shunt jumper, or by applying a wire between the option pads.

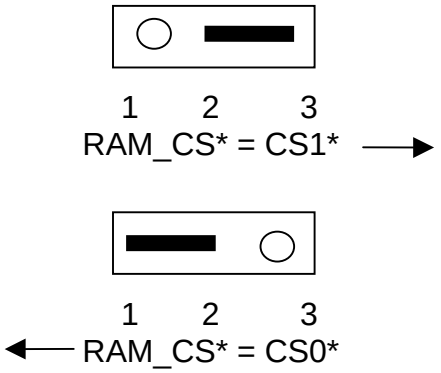
CONFIG SWITCH

The CONFIG switch provides reset configuration options for the MPC5554 device. Configuration options are enabled by position 1 of the switch. Switch positions 2 – 6 provide an active low output condition to the respective configuration signal and switch position on will provide an active high signal condition.

POSITION	CONFIGURATION SIGNAL	DESCRIPTION
6	WKPCFG	**ON = default**, Refer to Freescale MPC5554 Documentation
5	PLLCFG1	**OFF = default**, Refer to Freescale MPC5554 Documentation
4	PLLCFG0	**ON = default**, Refer to Freescale MPC5554 Documentation
3	BOOTCFG1	**OFF = default**, Refer to Freescale MPC5554 Documentation
2	BOOTCFG0	**OFF = default**, Refer to Freescale MPC5554 Documentation
1	CONFIG enable	**OFF= default.** ON = enables the RCON configuration to be applied from the switch settings.

SRAM_SEL Option

SRAM_SEL provides selection of the CS0 or CS1 chip selects to access the external SRAM (U2) on the DEMO board. The U2 device is a ISSI IS61SF12832 SRAM organized as 128K x 32 bits. Chip select configuration should be set for 0 wait states, 512K byte memory range, WE signals = Write Enable. The SRAM supports 4 word BURST mode access also.



POWER SUPPLY

This section covers the MPC5554DEMO board power supplies and options. The primary power supply is the MC33730 device configured to support the MPC5554 device. The MPC5554 VRC regulator provides the VDD (1.5V) supply in the default configuration (CT1 and CT4 Open, CT2 and CT3 closed). MC33730 1.5V supply may be applied by optional configuration to provide the VDD 1.5V supply (CT1 and CT4 closed, CT2 and CT3 open).

Power supply Reset signals for the 5V, 1.5V and 3.3V supplies are applied to the MPC5554 RESET* input by the closed S1 – S3 option pads respectfully. The open S0 option pad may apply the RSTKAM* back-up supply reset signal if closed by the user. Also see the POWER_PORT connection and MC33730 data sheet for power supply access details.

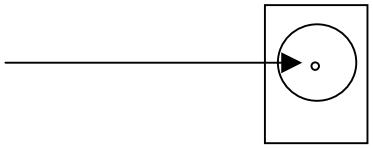
ON_OFF Switch

The ON_OFF toggle switch provides ignition on and off control to the MC33730 supply. The MC33730 device will enable and disable the main power supplies. With the switch in the ON position, all power indicators should light. Inspect input power connection and source, and fuse F1 if power indication does not occur.

PWR - Power Jack

The Power Jack provides the default power input to the board. The jack accepts a standard 2.0 ~ 2.1mm center barrel plug connector (positive voltage center) to provide the +VIN supply of +6 to +24 VDC (+12VDC typical).

+Volts, 2mm center



FUSE – F1

Input power is limited by fuse F1. An 5x20mm type 1A slow-blow type fuse is applied to protect the DEMO board for overload conditions.

Power Port

Power Port provides access to the main power supplies and MC33730 optional supplies. Note that the +VIN connection provided at pin 1 is not switched by the ON-OFF switch or fused and is directly connected to the Power Jack.

PIN #		SIGNAL DESCRIPTION
1	2	+V IN= DC input voltage from PWR jack (NO fuse or polarity protection).
3	4	+5V = regulated +5V supply from MC33730
5	6	+3.3V = regulated +3.3V supply from MC33730
7	8	+1.5V = regulated +1.5V supply from MC33730
9	10	VDD = MPC5554 VDD supply, 1.5V typically
11		VREF1 = MC33730 Optional 5V reference supply.
	12	+5VA = MC33730 VREF2 output dedicated to the MPC5554 5V analog supply.
13		RST3* = 3.3V power supply reset signal from MC33730 supply.
	14	VSTBY = 1V backup / standby voltage applied to MPC55554 VSTBY input. See VSTBY_SW and CT15 option also.
15		RSTL* = 1.5V power supply reset signal from MC33730 supply.
	16	REGON = control signal to the M33730, see MC33730 user guide.
17		RSTH* = 5V power supply reset signal from MC33730 supply.
	18	IGN_ON = control signal output from the MC33730, see MC33730 user guide.
19		RSTKAM* = Keep Alive / VSTBY / backup power supply reset signal from the MC33730.
	20	PFD = control signal output from the MC33730, see MC33730 user guide.
21	22	Ground / VSS

VSTBY SWITCH and CT15

The VSTBY SWITCH provides enabling and disabling the VSTBY operation of the MPC5554 internal RAM. Switch in the OFF position disables the VSTBY operation and the VSTBY pin is connected to VSS / Ground. Switch in the ON position applies the +1VDC VKAM standby voltage from the MC33730 supply to the VSTBY pin.

Cut-away option CT15 allows the user to isolate the VSTBY pin of the MPC5554 from the switch. With CT15 open, the user must apply external battery or ground to the VSTBY position on the Power Port connector or I/O header ring.

ANALOG SUPPLIES

The MPC5554 VDDA supply (+5V default) is provided by the MC33730 VREF2 regulator output. VRH reference supply is provided by VDDA by default with the VRH_EN option jumper installed. External VRH reference may be applied by removing the VRH_EN option and applying reference voltage at header ring I/O pin A9. The VRL_EN closed option pads connect the signal to common VSS supply by default. User may open this option to apply a precision ground to the VRL signal.

The QADC digital supply is provided +5V by option CT19. An optional connection to +3.3V for the QADC is provided by CT20. CT19 must be opened to install CT20 for +3.3V operation. See the MPC5554 user manual for more details on operating the QADC at +3.3V and limitations of the VDDA and VRH supplies.

USER COMPONENTS

The DEMO board provides External clock, 8 LED indicators, an 8 position DIP switch, 4 push switches, a speaker with amplifier, and 2 user potentiometers. These devices are accessed via the USER LED, USER SWITCH, and USER DEV I/O headers. DEMO board user may apply the devices to the MPC5554 I/O header signals to evaluate operation or assist in code development.

X1 CLOCK OSCILLATOR

The X1 socket is provided to install standard 5V compatible CAN type clock oscillators so that alternate clock source or frequencies maybe applied to the MPC5554. User should refer to the MPC5554 device user manual for information on frequency selection and clocking configuration.

X1 clock signal is provided to the MPC5554 by option pad set CT16 being closed by 0 ohm resistor or mod wire application. CUT-AWAY option CT5 must be opened to remove the Y1 crystal from the EXTAL signal or problems may occur with operation. User should review the MPC5554 user guide for proper PLLCFG0 and PLLCFG1 (CONFIG Switch 4 and 5) option settings if an external clock is applied.

USER_LED

User LED connector provides access to the user LED 1 to 8. Connector pins 1 to 8 are organized in a one to one connection to the individual indicators LED 1 to 8. The LED indicators are buffered for minimal drive current requirement (~300ua). Indicators will turn on with a logic high signal level of 2.5 to 5V applied at the respective connector pin.

USER_SWITCH

User Switch provides access to the 8 position User DIP Switch. Connector pins 1 to 8 organization provide a one to one organization to the individual DIP switch positions 1 to 8. The switch connections are pulled low with 10K ohm resistors when the switch position in the off position. Switch positions placed in the ON position will provide a 3.3V output to the connector.

USER_DEV

User DEV provides access to the 4 push switches (SW1 – SW4), speaker, and 2 user potentiometers (RV1 and RV2).

PIN #	USER COMPONENT CONNECTION
1	SW1 out, de-bounced CMOS drive 0 or 3.3V, active low.
2	SW1 out, de-bounced Open Drain output, active low, 10K ohm pull-up to 3.3V. Suitable for IRQ input signal drive.
3	SW2 out, active low, 10K ohm pull-up to 3.3V.
4	SW3 out, active low, 10K ohm pull-up to 3.3V.
5	SW4 out, active low, 10K ohm pull-up to 3.3V.
6	SPEAKER amp input. 0 to 5Vpp, volume adjust with SPKR_VOL.
7	RV1 center tap, 0 – 5V adjustment
8	RV2 center tap, 0 – 5V adjustment

SW1 – SW4 Push Switches

The push switches provide momentary active low input for user applications. SW1 has additional features of being de-bounced for no glitch operation and push-pull output on pin 1 or open drain output on pin 2. Typical user application would be to provide program control or menu selection input.

RV1 and RV2 User Potentiometers

The User Potentiometers provide an adjustable linear voltage output from 0 to 5V. The voltage signal may be applied to an MPC5554 analog input port for user application.

SPEAKER and SPKR_VOL

The speaker and amplifier provide user applications with a method to generate sound effects from a MPC5554 output. Frequency range of the amplifier input is 300Hz to 10Khz. The SPKR_VOL potentiometer allows user adjustment of the sound effect volume from the speaker. The amplifier also provides a SHDN input connection pad. This pad maybe connected to a MPC5554 output signal to disable the amplifier with a logic high signal of 3.3V or 5V.

COM-1 PORT

COM-1 is a standard RS232 type serial port configured for direct connection to a PC COM Port with a straight through type 9 pin serial cable. Option JP1 provides MPC5554 SCI channel 'A' signal connections when installed. Optional RTS and CTS hardware flow control connection pads are provided for the user to apply MPC5554 I/O ports and software to enhance operation.

JP1 Option

The JP1 Option provides MPC5554 RXDA and TXDA signals to the COM1 transceiver connections. This allows the user to apply the provided communication transceiver with the SCI A channel or to apply the associated I/O to other purposes. JP1 position 1 installed enables the TXDA output and position 2 enables the RXDA input on COM-1.

COM1

1	**1**		X
TXD	**2**	**6**	6
RXD	**3**	**7**	CTS IN
4	**4**	**8**	RTS OUT
GND	**5**	**9**	9

The **COM-1** port is a Female (socket type) DB9 connector.

Pins 1, 4, and 6 connected for status null to host.

Pins 7 and 8 maybe applied by CTS and RTS pads to MPC5554 I/O.

RTS signal active output level is logic 0. User should place I/O port applied at logic low (0) to enable the RTS signal and reception of bytes if applied. User should apply a logic high signal under software control inform host or connected RS232 device to STOP transmitting (stop sending incoming bytes).

CTS signal active input is level is logic 0. User should apply software to detect a logic high signal or rising edge on applied I/O port and STOP transmitting bytes to the host or connected device to implement hardware flow control. Detection of a logic low input indicates the host is ready to receive bytes and the user may transmit.

DB9 connector pin locations are provided access pads behind the connector on the DEMO board. User may isolate the connection pads by cutting the associated circuit trace on the bottom of the board.

CAN_PORT

The CAN Port provides 9 pin connector with a TJA1050 CAN transceiver interface to the MPC5554 CAN channels. The CAN_SEL option locations select the CAN channel applied to the transceiver and CAN Port. User may apply more than one MPC5554 CAN channel to the port if the open drain TX output type is applied on the associated CAN channel transmit pins.

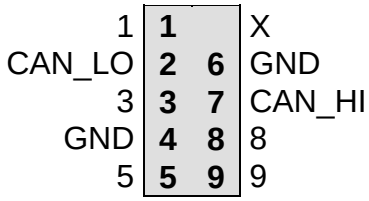
CAN_SEL Option

The CAN_SEL option header allows selection of the MPC5554 CAN channels applied to the CAN transceiver and CAN Port. If more that one transmit channel is applied, the open drain output feature of the transmit pins must also be applied.

POSITION #	MPC5554 CAN SIGNAL
1	CNTX_A, channel A TX out (**DEFAULT enabled**)
2	CNRX_A, channel A RX in (**DEFAULT enabled**)
3	CNTX_B, channel B TX out
4	CNRX_B, channel B RX in
5	CNTX_C, channel C TX out
6	CNRX_C, channel C RX in

Following is the DB9S connection reference.

CAN_PORT



CAN port has a Female (socket type) DB9 connector.

CAN_HI and CAN_LO signals are terminated together with 120 ohms (R68).

DB9 connector pin locations are provided access pads behind the connector on the DEMO board for additional user application.

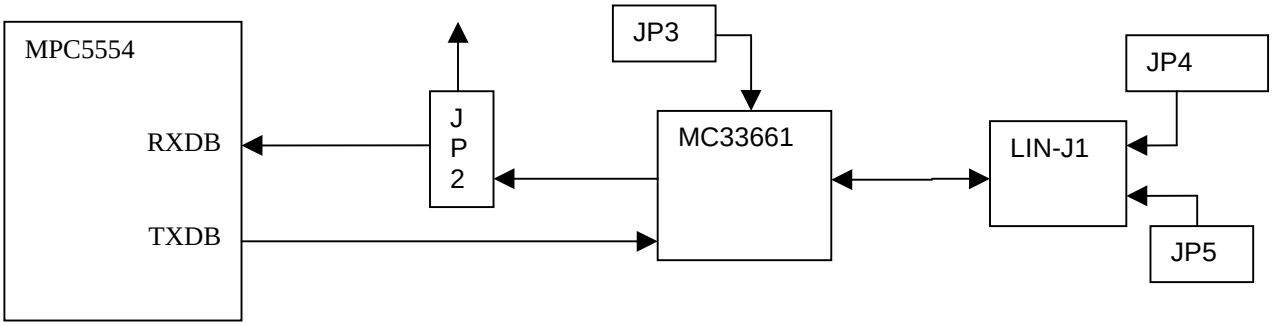
JP7 Option

JP7 provides user option access to the CAN transceiver control input. Default option position of 1-2 selected provides normal CAN transceiver operation. User may option CAN transceiver for Transmit control by moving JP7 option jumper to positions 2-3 and applying a MPC5554 output pin to JP7 pin 1. Transmit disable operation is active high.

LIN_J1

The LIN_J1 port provides a Master Mode LIN network connection. The MPC5554 device provides a LIN Master type node on the LIN Network. A LIN physical layer transceiver U7 (MC33661, or similar) is provided between the MPC5554 device and the LIN network connector. Refer to the MC33661 data sheet for complete details of transceiver operation.

The following diagram represents the LIN connection:



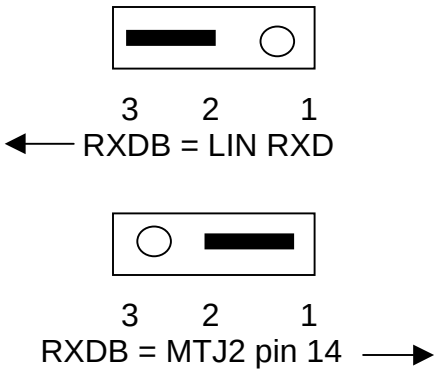
The LIN interface provides optional features of slew rate control, network supply, and wake up option. See the JP2, JP3, JP4, JP5 and CT17 options following.

CT17 Option

MPC5554 I/O signal GPIO205 provides LIN transceiver U7 enable control (EN pin). Software control of the EN pin allows the user to set the slew rate control of the transceiver. User applications should configure the GPIO205 pin for output to operate the LIN transceiver. If GPIO205 is needed for other purposes, the CT17 option maybe cut to isolate the signal from the LIN transceiver. Refer to the MC33361 data sheet for further details of operation.

JP2 Option

JP2 selects the MPC5554 SCI RXDB signal source to be from the LIN transceiver or MTJ2 target board connector. For LIN operation JP2 must be in the 1 – 2 position.

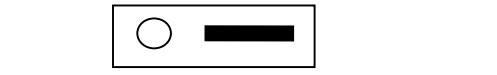


JP3 Option

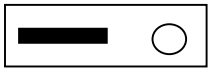
Installation of JP3 applies a pull-up resistor on the LIN transceiver enable pin. MPC5554 GPIO205 may still control the transceiver enable operation when JP3 is installed.

JP4 Option

LIN-J1 connector pin 2 may be configured for different network requirements by JP4. JP4 open will disconnect LIN-J1 pin 2 from the DEMO board.



LIN-J1 pin 2 = Ground / VSS ⟶



⟵ LIN-J1 pin 2 = Transceiver WAKE pin

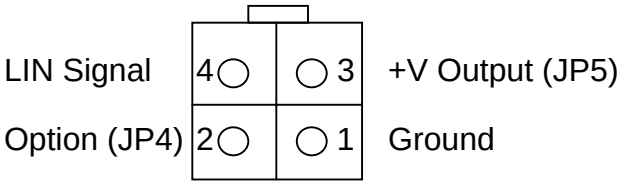
JP5 Option

Installation of JP5 applies LIN network power to LIN-J1 pin 3 from the MPC5554DEMO board +VIN input. This connection allows the DEMO board as a LIN master node to power remote LIN slave nodes. User should use caution verify only one source is applied on the network.

LIN-J1 Connector

The LIN-J1 network connector provides a standard pin configuration with a network option position on pin 2.

Front view (looking into connector from outside of board edge)



Mating connector = Molex 39-01-2040 with 39-00-0039 pins.

DEVELOPMENT PORTS

The MPC5554DEMO board provides 1 JTAG and 2 NEXUS type development ports. Only one of the development ports should be applied due to common signals used on the ports. The development port input and power signals are buffered by a CBTLV3861 device. This buffer provides a bi-directional 5 ohms series resistance on the input signals when powered on. The buffer also provides signal isolation when powered off.

NOTE: Proper power sequencing must be performed when a development port is applied (cable connected). Development port application power sequence:
1) MPC5554DEMO board ON–OFF switch is OFF and no power is applied to the PWR connector.
2) Connect development port cable to the desired MPC5554DEMO board development port.
3) Apply power to the MPC5554DEMO board PWR connector and turn ON–OFF switch ON.
4) If power is removed or the ON-OFF switch is turned off, remove development cable from board connector and re-apply from step 1 of this procedure.

NEXUS Port

The NEXUS port provides a more powerful and higher speed development port for high end tools. The port connector is an AMP 38 pin Mictor style, part number #767054-1.

NEXUS Port

Signal	Pin #	Pin #	Signal
NXS1 TP	1	2	NXS2 TP
NXS3 TP	3	4	NXS4 TP
MDO9	5	6	CLKOUT
BOOTCFG1	7	8	MDO8
B_RESET*	9	10	B_EVTI*
TDO	11	12	B_+3.3V
MDO10	13	14	B_RDY*
B_TCK	15	16	MDO7
B_TMS	17	18	MDO6
B_TDI	19	20	MDO5
B_JCOMP	21	22	MDO4
MDO11	23	24	MDO3
ERSTOUT*	25	26	MDO2
NXS27 TP	27	28	MDO1
NXS29 TP (Note 3)	29	30	MDO0
+V	31	32	EVTO*
+V	33	34	MCKO
NXS35 TP (Note 3)	35	36	MSEO1*
B_VSTBY	37	38	MSEO0*

Notes:
1) B_… signals are buffered.
2) NXSxx TP signals are not connected to the MPC554 and provide a Test Pad on the board.
3) NXSxx signal TP is also connected to the ROBUST Nexus connector.
4) Signals followed by a “*” symbol are active logic low.

JTAG Port

The JTAG port provides a Freescale standard JTAG connection to the MPC5554. The connector is a standard 2x7, .1 inch pin space keyed pin header. Example compatible cables include the OCDEMON™ NP-JTAG ONCE "Wiggler" and the P&E Microcomputer Systems CABPPCNEXUS. Host software must be applied to operate the cables.

JTAG Port

Signal	Pin #	Pin #	Signal
B_TDI	1	2	GND
TDO	3	4	GND
B-TCK	5	6	GND
B_EVTI*	7	8	JTG8 TP
B-RESET*	9	10	B_TMS
B_+3.3V	11	12	GND
B_RDY*	13	14	B_JCOMP

Notes:
1) B_… signals are buffered.
2) JTG8 TP signal is not connected to the MPC5554 and provides a Test Pad on the board.
3) Pin 7 or the B_EVTI* signal may not be supported by all development cables. Option CT18 cut will isolate this signal if not supported by the development cable and issues are present.
4) Signals followed by a "*" symbol are active logic low.

ROBUST Port

The ROBUST port connector location is provided for user expansion. This port provides the ROBUST Nexus 51 pin location that applies the GLENAIR MR7580-51P2BNU connector.

ROBUST Port

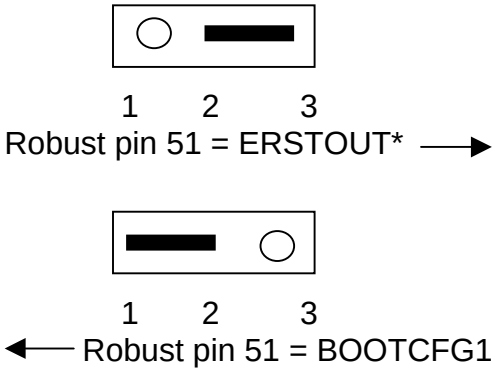
Pin #	Signal	Pin #	Signal	Pin #	Signal
1	+V	19	MDO0	36	GND
2	+V	20	GND	37	MDO4
3	B_VSTBY1	21	MCKO	38	GND
4	NXS35 TP	22	GND	39	MDO5
5	TDO	23	EVTO*	40	GND
6	B_RDY*	24	GND	41	MDO6
7	B_RESET*	25	MSEO0*	42	GND
8	B_+3.3V	26	MDO9	43	MDO7
9	B_EVTI*	27	MDO1	44	GND
10	GND	28	GND	45	MDO8
11	B_JCOMP	29	MDO2	46	GND
12	GND	30	GND	47	MDO10
13	B_TMS	31	MDO3	48	GND
14	GND	32	GND	49	MDO11
15	B_TDI	33	NXS29 TP	50	GND
16	GND	34	GND	51	JP6 pin 2
17	B_TCK	35	MSEO1*		
18	GND				

Notes:
1) NXS29 and NXS35 signals are also connected to the NEXUS connector.

2) Signals followed by a "*" symbol are active logic low.

JP6 Option

JP6 provides signal selection for the Robust Nexus connector pin 51. Position 1-2 provides the BOOTCFG1 signal and position 2-3 provides the ERSTOUT* signal.



MT_J1/2/3 Ports

The MT_Jx ports are provided for easy expansion and interface to the MCU_TARGET application board. Features on the MCU_TARGET board allow additional demonstration of MPC5554 applications without adding prototype hardware to the MPC5554DEMO board.

A 20 position standard female ribbon cable can be applied to the connectors for interface to the MCU_TARGET board or other platform. The connectors may also be applied for other purposes.

MT_J1

MPC5554 Signal	Pin #	Pin #	MPC5554 Signal
GND	1	2	GND
AN32	3	4	TPU_A28
AN33	5	6	TPU_A29
	7	8	EMIOS23
	9	10	TPU_A30
AN34	11	12	TPU_A31
AN35	13	14	AN37
TPU_A27	15	16	AN38
AN36	17	18	
AN39	19	20	

MT_J2

MPC5554 Signal	Pin #	Pin #	MPC5554 Signal
	1	2	GND
SOUT_B	3	4	1K GND
SIN_B	5	6	PCS_B3
SCK_B	7	8	1K GND
PCS_B0	9	10	PCS_B4
PCS_B1	11	12	
PCS_B2	13	14	MTJ2_RXD
TCRCLK_A	15	16	TXDB
	17	18	
	19	20	

MT_J2 NOTE: Pin 14 / MTJ2_RXD is applied to MPC5554 RXDB via option jumper JP2.

MT_J3

MPC5554 Signal	Pin #	Pin #	MPC5554 Signal
GND	1	2	GND
TPU_B25	3	4	
TPU_B26	5	6	
TPU_B27	7	8	
TPU_B28	9	10	
TPU_B29	11	12	
TPU_B30	13	14	
TPU_B31	15	16	
TPU_B24	17	18	
TCRCLK_B	19	20	

MT_J3 NOTE: Pins 11, 13, and 15 have a 1K ohm series resistance to the MPC5554 I/O pin.

MPC5554 I/O HEADER RING

MPC5554 I/O signals are provided by the I/O header ring. The header ring consists of .1 inch grid pins organized in 4 rows for each side of the MPC5554 device. Each row reflects the corresponding location of the MPC5554 device BGA ball ring.

A1 – AF4 HEADER

BALL - SIGNAL	BALL - SIGNAL	BALL – SIGNAL	BALL - SIGNAL
A1 – GND	A2 – VSTBY	A3 – AN37	A4 – AN11
B1 – VDD	B2 – GND	B3 – AN36	B4 – AN39
C1 – 3.3V	C2 – VDD	C3 – GND	C4 – AN8
D1 – TPU_A30	D2 – TPU_A31	D3 – VDD	D4 – GND
E1 – TPU_A28	E2 – TPU_A29	E3 – 5V	E4 – VDD
F1 – TPU_A24	F2 – TPU_A27	F3 – TPU_A26	F4 – 5V
G1 – TPU_A23	G2 – TPU_A22	G3 – TPU_A25	G4 – TPU_A21
H1 – TPU_A20	H2 – TPU_A19	H3 – TPU_A18	H4 – TPU_A17
J1 – TPU_A16	J2– TPU_A15	J3– TPU_A14	J4– TPU_A13
K1 – TPU_A12	K2 – TPU_A11	K3 – TPU_A10	K4 – TPU_A9
L1 – TPU_A8	L2 – TPU_A7	L3– TPU_A6	L4– TPU_A5
M1 – TPU_A4	M2 – TPU_A3	M3 – TPU_A2	M4 – TPU_A1
N1 – BDIP*	N2 – TEA*	N3 – TPU_A0	N4 – TCRCLK_A
P1 – CS3*	P2 – CS2*	P3 – CS1*	P4 – CS0*
R1 – WE3*	R2 – WE2*	R3 – WE1*	R4 – WE0*
T1 – 3.3V	T2 – TSIZ0	T3 – RD_WR	T4 – 3.3V
U1 – A16	U2 – TSIZ1	U3 – TA*	U4 – 3.3V
V1 – A18	V2 – A17	V3 – TS*	V4 – A8
W1 – A20	W2 – A19	W3 – A9	W4 – A10
Y1 – A22	Y2 – A21	Y3 – A11	Y4 – 3.3V
AA1 – A24	AA2 – A23	AA3 – A13	AA4 – A12
AB1 – 3.3V	AB2 – A25	AB3 – A15	AB4 – A14
AC1 – A26	AC2 – A27	AC3 – A31	AC4 – GND
AD1 – A28	AD2 – A30	AD3 – GND	AD4 – VDD
AE1 – A29	AE2 – GND	AE3 – VDD	AE4 – D17
AF1 - GND	AF2 - VDD	AF3 – D16	AF4 – D18

A5 – D22 HEADER

BALL - SIGNAL	BALL – SIGNAL	BALL – SIGNAL	BALL - SIGNAL
A5 – VDDA	B5 – AN19	C5 – AN17	D5 – AN38
A6 – AN16	B6 – AN20	C6 – VSSA	D6 – AN9
A7 – AN1_AND0-	B7 – AN0_AND0+	C7 – AN21	D7 – AN10
A8 – AN5_AND2-	B8 – AN4_AND2+	C8 – AN3_DAN1-	D8 – AN18
A9 – VRH	No Connection	C9 – AN7_DAN3-	D9 – AN2_DAN1+
A10 – AN23	B10 – AN22	C10 – VRL	D10 – AN6_DAN3+
A11 – AN27	B11 – AN26	C11 – AN25	D11 – AN24
A12 – AN28	B12 – AN31	C12 – AN30	D12 – AN29
A13 – AN35	B13 – AN32	C13 – AN33	D13 – AN34
A14 – GND	B14 – GND	C14 – 5V	D14 – 5V
A15 – AN15	B15 – AN14	C15 – AN13	D15 – AN12
A16 – ETRIG1	B16 – ETRIG0	C16 – TPU_B19	D16 – TPU_B16
A17 – TPU_B18	B17 – TPU_B21	C17 – TPU_B22	D17 – TPU_B17
A18 – TPU_B20	B18 – TPU_B25	C18 – TPU_B26	D18 – TPU_B23
A19 – TPU_B24	B19 – TPU_B28	C19 – TPU_B30	D19 – TPU_B29
A20 – TPU_B27	B20 – TPU_B31	C20 – MDO9	D20 – MDO5
A21 – GPIO205	B21 – MDO10	C21 – MDO6	D21 – MDO2
A22 – MDO11	B22 – MDO7	C22 – MDO3	D22 – 5V

A23– AF26 HEADER

BALL - SIGNAL	BALL - SIGNAL	BALL – SIGNAL	BALL - SIGNAL
A23 – MDO8	A24 – VDD	A25 – 3.3V	A26 – GND
B23 – MDO4	B24 – MDO0	B25 – GND	B26 – 3.3V
C23 – MDO1	C24 – GND	C25 – 3.3V	C26 – VDD
D23 – GND	D24 – 3.3V	D25 – TCK	D26 – TDI
E23 – 3.3V	E24 – TMS	E25 – TDO	E26 – TEST*
F23 – MSEO0*	F24 – JCOMP	F25 – EVTI*	F26 – EVTO*
G23 – MSEO1*	G24 – MCKO	G25 – GPIO204	G26 – TPU_B15
H23 – RDY*	H24 – GPIO203	H25 – TPU_B14	H26 – TPU_B13
J23 – 5V	J24 – TPU_B12	J25- TPU_B11	J26 – TPU_B9
K23 – TPU_B10	K24 – TPU_B8	K25 – TPU_B7	K26 – TPU_B5
L23 – TPU_B6	L24 – TPU_B4	L25 – TPU_B3	L26 – TPU_B2
M23 – TCRCLK_B	M24 – TPU_B1	M25 – TPU_B0	M26 – SIN_B
N23 – SOUT_B	N24 – PCS_B3	N25 – PCS_B0	N26 – PCS_B1
P23 – PCS_A3	P24 – PCS_B4	P25 – SCK_B	P26 – PCS_B2
R23 – PCS_B5	R24 – SOUT_A	R25 – SIN_A	R26 – SCK_A
T23 – PCS_A1	T24 – PCS_A0	T25 – PCS_A2	T26 – 5V
U23 – PCS_A4	U24 – TXDA	U25 – PCS_A5	U26 – 3.3V
V23 – CNTX_C	V24 – RXDA	V25 – RSTOUT*	V26 – RSTCFG*
W23 – RXDB	W24 – CNRX_C	W25 – TXDB	W26 – RESET*
Y23 – WKPCFG	Y24 – BOOTCFG1	Y25 – GND	Y26 – GND
AA23 – 5V	AA24 – PLLCFG1	AA25 – BOOTCFG0	no connection
AB23 – VDD	no connection	AB25 – PLLCFG0	no connection
AC23 – GND	AC24 – VDD	AC25 – VRC33	no connection
AD23 – NC1	AD24 – GND	AD25 – VDD	AD26 – 3.3V
AE23 – 3.3V	AE24 – CLKOUT	AE25 – GND	AE26 – VDD
AF23 – CNRX_B	AF24 – 3.3V	AF25 - ENGCLK	AF26 - GND

AC5 – AF22 HEADER

BALL - SIGNAL	BALL - SIGNAL	BALL – SIGNAL	BALL - SIGNAL
AC5 – VDD	AD5 – D24	AE5 – D19	AF5 – 3.3V
AC6 – D26	AD6 – D25	AE6 – D21	AF6 – D20
AC7 – D28	AD7 – D27	AE7 – D23	AF7 – D22
AC8 – 3.3V	AD8 – D29	AE8 – D0	AF8 – GPIO206
AC9 – D30	AD9 – 3.3V	AE9 – D2	AF9 – D1
AC10 –D31	AD10 – GPIO207	AE10 –D4	AF10 –D3
AC11 – D8	AD11 – D9	AE11 – D6	AF11 – 3.3V
AC12 – D10	AD12 – D11	AE12 – OE*	AF12 – D5
AC13 – 3.3V	AD13 – D13	AE13 – BR*	AF13 – D7
AC14 – D12	AD14 – D15	AE14 – BG*	AF14 – BB*
AC15 – D14	AD15 – EMIOS3	AE15 – EMIOS1	AF15 – EMOS0
AC16 – EMIOS2	AD16 – EMIOS6	AE16 – EMIOS5	AF16 – EMIOS4
AC17 – EMIOS8	AD17 – EMIOS10	AE17 – EMIOS9	AF17 – EMIOS7
AC18 – EMIOS12	AD18 – EMIOS15	AE18 – EMIOS13	AF18 – EMIOS11
AC19 – EMIOS21	AD19 – EMIOS17	AE19 – EMIOS16	AF19 – EMIOS14
AC20 – 5V	AD20 – EMIOS22	AE20 – EMIOS19	AF20 – EMIOS18
AC21 – 3.3V	AD21 – CNTX_A	AE21 – EMIOS23	AF21 – EMIOS20
AC22 – NC1	AD22 – 3.3V	AE22 – CNRX_A	AF22 – CNTX_B

Note: Indicated as AD5 / AF5 on DEMO board.